Techno India NJR Institute of Technology

Course File

Session 2020-21

VLSI Design (5EX5-13)

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(Assistant Professor)
Department of ECE

For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
(Principal)

RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Syllabus

III Year - V Semester: B.Tech. (Electrical And Electronics Engineering)

5EX5-13: INTRODUCTION TO VLSI

Credit: 2 **Max. Marks: 100(IA:20, ETE:80)**
2L+0T+0P **End Term Exam: 2 Hours**

SN	CONTENTS	HOURS
1	**Introduction:** Objective, scope and outcome of the course.	01
2	**Introduction to MOS Technology:** Basic MOS transistors, Enhancement Mode transistoraction, Depletion Mode transistor action, NMOS and CMOS fabrication.	06
3	**Basic Electrical Properties of MOS Circuits:** IDS versus VDS relationship, Aspects of threshold voltage, Transistor Trans conductance gm. The NMOS inverter, Pull up to Pull-down ratio for a NMOS Inverter and CMOS Inverter (Bn/Bp), MOS transistor circuit Model, Noise Margin.	05
4	**CMOS Logic Circuits:** The inverter, Combinational Logic, NAND Gate NOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers Transmission Gate, Gate delays, CMOS-Gate Transistor sizing, Power dissipation	06
5	**Basic Physical Design of Simple Gates and Layout Issues:** Layout issues for inverter, Layout for NAND and NOR Gates, Complex Logic gates Layout, Layout optimization for performance.	06
6.	**Introduction to VHDL:** Verilog & other design tools. VHDL Code for simple Logic gates, flip-flops, shift-registers, Counters, Multiplexers, adders and subtractors.	03
	TOTAL	27

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Course Overview:

Student will learn fundamentals of VLSI design from this 40-hour course. In this course, student will study the fundamental concepts and structures of designing digital VLSI systems include CMOS devices and circuits, standard CMOS fabrication processes, CMOS design rules, static and dynamic logic structures, interconnect analysis, CMOS chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture.

Course Outcomes:

CO.NO.	Cognitive Level	Course Outcome
1	Analysis	Analyse and Simulate MOS Inverter characteristics.
2	Synthesis	Explain various dynamic MOS circuits.
3	Synthesis	Comprehend and design Semiconductor Memories.

Prerequisites:

1. Fundamentals of semiconductor devices.
2. Must have completed the course on Digital and Analog Electronics.
3. Student should be able to design any digital circuit for given requirements.

Course Outcome Mapping with Program Outcome:

Course Outcome	Program Outcomes (PO's)											
CO. NO.	Domain Specific					Domain Independent						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	1		2	0						
CO2	2	2	2	2	2	1						
CO3	2	3	2	2	2	1						
1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High)												

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Course Coverage Module Wise:

Lecture No.	Unit	Topic
1	**1**	**INTRODUCTION TO MOSFET**
2	1	Basic MOS transistors, Enhancement Mode transistor action, Depletion Mode transistor action.
3	1	NMOS and CMOS fabrication.
4	1	Aspects of threshold voltage, threshold voltage with body effect.
5	1	Ids versus Vds relationship, channel length modulation, Transistor Trans-conductance gm
6	1	MOS transistor circuit Model.
7	1	Model parameter (oxide and junction capacitor, channel resistance) variation with scaling and biasing.
8	1	High order effects
9	1	Sub-threshold conduction & hot electron effect,
10	1	Narrow channel effect and punch through effect.
11	**2**	**CMOS LOGIC CIRCUITS**
12	2	nMOS inverter (resistive and active load)
13	2	Pull up to Pull-down ratio for a NMOS Inverter
14	2	CMOS Inverter & Pull up to Pull-down ratio (Bn/Bp).
15	2	determination of inverter parameter (VIL, VIH VOL VOH)
16	2	Noise Margin. Speed and power dissipation analysis of CMOS inverter
17	2	Combinational Logic, NAND Gate, NOR gate, XOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers.
18	2	Transmission Gate, estimation of Gate delays, Power dissipation and Transistor sizing.
19	**3**	**BASIC PHYSICAL DESIGN OF SIMPLE GATES AND LAYOUT ISSUES**
20	3	Layout issues for CMOS inverter
21	3	Layout for NAND, NOR and Complex Logic gates
22	3	Layout of TG.
23	3	Layout optimization using Eular path.
24	3	DRC rules for layout
25	3	issues of interconnects
26	3	Latch up problem.
27	**4**	**DYNAMIC CMOS CIRCUITS**
28	4	Clocked CMOS (C2MOS) logic
29	4	DOMINO logic
30	4	NORA logic.
31	4	NP(ZIPPER) logic
32	4	PE(pre-charge and Evaluation) Logic
33	4	Basic Memory circuits
34	4	SRAM and DRAM
35	**5**	**PHYSICAL DESIGN**
36	5	Introduction to ECAD tools for front and back end design

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37	5	Custom /ASIC design
38	5	Design using FPGA & VHDL
39	5	VHDL Code for simple Logic gates
40	5	VHDL Code for flip-flops, shift registers

TEXT/REFERENCE BOOKS

1. CMOS Digital Integrated Circuits Analysis and Design, Sung Mo Kang and Yusuf Leblebici, McGraw-Hill
2. Principles of CMOS VLSI Design, Neil H.E Weste and Kamran Eshraghian, Pearson Education LPE
3. Basic of VLSI Design, A. Douglas Puchnell & Kamran Eshraghian, PHI

Teaching and Learning resources:

- **MOOC (NPTEL): -** https://nptel.ac.in/courses/108/107/108107129/

Assessment Methodology:

1. Practical exam using Microwind VLSI design software.
2. Two Midterm exams where student have to showcase subjective learning.
3. Final Exam (subjective paper) at the end of the semester.

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7E7084

Roll No. _____ Total No. of Pages : 2

7E7084

B.Tech. VII- Semester (Main&Back) Examination, November - 2019
Electronics and Comm. Engg.
7EC5A VLSI Design

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly) Units of quantities used/calculated must be stated clearly.

UNIT - I

1. a) Develop the relation between I_{ds} and V_{ds} for MOSFET and modify it under channel length modulation. **(8)**

   b) Draw variation of gate oxide capacitance with V_{ds}. Assume the gate voltage $V_{gs} > V_{th}$. **(6)**

   c) State the condition of ohmic operation. **(2)**

OR

1. a) Find the expression of threshold voltage V_{so} and discuss how it modified under body bias. **(8)**

   b) Discuss any two phenomena in MOSFET from.

   i) Hot electron effect

   ii) Subthreshold conduction

   iii) Narrow channel effect. **(4+4=8)**

UNIT - II

2. a) Draw NMOS inverter with active load and draw its Transfer characteristic. Also find the expression 7 V_{IL}, V_{INV}, V_{OL} and V_{OH} for it. **(10)**

   b) Draw $y = A + \overline{BC}$ using CMOS. **(6)**

OR

2. b) Draw and explain the working of Transmission gate (TG). Use it for 2×1 CMOS multiplexer. **(8)**

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b) What is transistor sizing? Design a y = ABC CMOS logic such that its equivalent (D/L) of pull up section is 90 and pull down section is 30. (8)

Unit - III

3. a) Draw following CMOS Ckt
   i. y = A+BC+D
   ii. $y = \overline{A} + \overline{BC}$ (4+4=8)
   b) Draw the layout of y = AB+CDE CMOS ckt use Eular path in it. (8)

OR

3. a) What is Latch up Problem? How it can be avoided in CMOS ckts? (8)
   b) State any four DRC rules regarding:
   i. Contact size
   ii. Metal to Metal line separation.
   iii. Poly width and
   iv. Separation between pdiff and Ndiff. (4×2=8)

Unit - IV

4. Draw and explain any two logic Ckt from.
   i. NORA logic.
   ii. DRAM
   iii. DOMINO logic
   iv. NP logic. (2×8=16)

Unit - V

5. Write short note on any two :
   i. VHDL code
   ii. FPGA
   iii. Custom design
   iv. ASIC design (2×8=16)

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Total No of Pages: 3

7E7084

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

UNIT- I

Q.1 (a) What are different kinds of MOS transistors? Explain the structure and operation of MOS transistor. [8]

(b) The process parameters for an NMOS are - [8]

Oxide thickness = 500 A° , Substrate doping $M_A = 10^{16}/cm^3$, Polysilicon gate doping $M_D = 10^{20}/cm^3$, Oxide interface fixed charge density = $2\times10^{10}/cm^3$. Calculate the threshold voltage V_T.

OR

Q.1 (a) What are the different techniques of CMOS transistor fabrication? Explain one in detail. [8]

(b) Explain "Depletion mode MOSFET". [8]

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UNIT- II

Q.2 (a) Write short note on – [8]

(i) Noise Margins

(ii) Pull-up to pull – down ratio for an NMOS inverter.

(b) Design a resistive load inverter with R = 1kΩ such that at V_{OL} = 0.6V. The enhancement type NMOS driver transistor has following parameters : V_{DD} = 5V, V_T = 1V, $\mu_n.C_{ox}$ = 22μ A/V² – [8]

(i) Determine the aspect ratio

(ii) Determine Noise margins NM_L and NM_H.

OR

Q.2 (a) Derive β_n/β_p ratio of CMOS inverter. [10]

(b) The NMOS device with V_t = 0.7V has its source terminal grounded and a 1.3V is applied to gate. The device has $\mu_n.C_{ox}$ = 100 mA/V², W = 10mm, L = 1mm. Find the value of drain current for V_D = 3V. [6]

UNIT- III

Q.3 (a) Realize the following expression using CMOS inverter – [8]

(i) $AB + \overline{A}\,\overline{B}$

(ii) $\overline{A + BC + DE}$

(iii) AB + BC + AC

(iv) A⊙B

(b) What are DRC rules for layout? State any six DRC rules. [8]

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OR

Q.3 (a) Draw the layout using Euler path for $y = \overline{(A+BC)(D+E)}$. [8]

(b) Draw latch – up formation in CMOS inverter. [8]

UNIT- IV

Q.4 (a) What is C^2 MOS logic? Draw logic circuit using it. What are advantages of such logic? [8]

(b) Explain the working of SRAM cell and DRAM cell. [8]

OR

Q.4 (a) Explain pre – charge and evaluation logic. [8]

(b) Draw $y = \overline{(AB+C)}$ using Domino logic. [8]

UNIT- V

Q.5 (a) Write VHDL Code for S – R flip flop and D-flip flop. [10]

(b) List the advantages and limitations of VHDL. [6]

OR

Q.5 (a) Write the difference between FPGA and custom design. [8]

(b) Write the difference between first and back end design. [8]

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