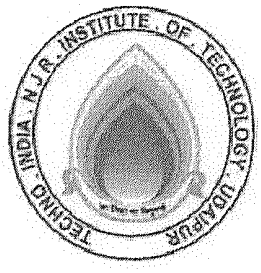
Techno India NJR Institute of Technology



Course File

Session 2021-22

Digital Electronics (3CS3-04)

Yogendra Singh Solanki
(Assistant Professor)
Department of ECE

For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
(Principal)

RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Syllabus

II Year-III Semester: B.Tech. Computer Science and Engineering

3CS3-04: Digital Electronics

Credit-3
3L+0T+0P

Max. Marks : 150 (IA:30,ETE:120)
End Term Exam: 3 Hours

SN	CONTENTS	Hours
1	**Fundamental concepts:** Number systems and codes, Basic logic Gates and Boolean algebra: Sign & magnitude representation, Fixed point representation, complement notation, various codes & arithmetic in different codes & their inter conversion. Features of logic algebra, postulates of Boolean algebra.Theorems of Boolean algebra.	8
2	**Minimization Techniques and Logic Gates:** Principle of Duality - Boolean expression -Minimization of Boolean expressions — Minterm – Maxterm - Sum of Products (SOP) – Product of Sums (POS) – Karnaugh map Minimization – Don't care conditions – Quine - McCluskey method of minimization.	8
3	**Digital Logic Gate Characteristics:** TTL logic gate characteristics. Theory & operation of TTL NAND gate circuitry. Open collector TTL. Three state output logic. TTL subfamilies.MOS& CMOS logic families. Realization of logic gates in RTL, DTL, ECL, C-MOS & MOSFET.	8
4	**Combinational Circuits:** Combinational logic circuit design, adder, subtractor, BCD adder encoder, decoder, BCD to 7-segment decoder, multiplexer demultiplexer.	8
5	**Sequential Circuits:** Latches, Flip-flops - SR, JK, D, T, and Master-Slave Characteristic table and equation,counters and their design, Synchronous counters – Synchronous Up/Down counters – Programmable counters – State table and state transition diagram ,sequential circuits design methodology, Registers –shift registers.	8
	TOTAL	40

Course Overview:

Digital circuits are part of any electronic design today. This also happens to be one of the core subjects for the undergraduate students in Electronics, Electrical and Computer Engineering. It forms the basis of many of the next level courses. The proposed course on digital circuits will cover all the fundamental concepts in digital design. The course will start with the representations of numbers – different number systems and conversion between them, representation of integer and real numbers etc. This will be followed by combinational and sequential circuit design techniques.

Course Outcomes:

CO.NO.	Cognitive Level	Course Outcome
1	Knowledge	Develop the understanding of number system and its application in digital electronics.
2	Application	Development and analysis of K-map to solve the Boolean function to the simplest form for the implementation of compact digital circuits.
3	Analysis	Acquire knowledge about various logic gates and logic families and analyze basic circuits of these families.
4	Synthesis	Develop ability to identify, analyze and design combinational circuits like half adder full adder, MUX, DEMUX encoder, decoder.
5	Synthesis	Develop ability to design various synchronous and asynchronous sequential circuits like registers FLIP FLOP, and counters.

Prerequisites:

1. Fundamentals of semiconductor devices& Boolean logics.

Course Outcome Mapping with Program Outcome:

Course Outcome	Program Outcomes (PO's)											
CO. NO.	Domain Specific					Domain Independent						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	0	0	1	0	0	0	0	1	0
CO2	1	1	1	2	0	0	2	0	0	0	0	0
CO3	2	1	2	1	1	1	0	0	0	0	1	1
CO4	1	1	2	1	1	0	0	0	0	0	1	0
CO5	1	1	2	1	1	0	0	0	0	0	1	0
1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High)												

Course Coverage Module Wise:

Lecture No.	Unit	Topic
1	1	**Fundamental concepts:** Number systems and codes,
2	1	Basic logic Gates and Boolean algebra
3	1	Sign & magnitude representation, Fixed point representation
4	1	Sign & magnitude representation, Fixed point representation
5	1	Complement notation, various codes & arithmetic in different codes &their inter conversion
6	1	Complement notation, various codes & arithmetic in different codes &their inter conversion
7	1	Features of logic algebra, postulates of Boolean algebra
8	1	Theorems of Boolean algebra
9	2	**Minimization Techniques and Logic Gates**: Principle of Duality
10	2	Boolean expression -Minimization of Boolean expressions
11	2	Minterm – Maxterm - Sum of Products (SOP) – Product of Sums (POS)
12	2	Karnaugh map Minimization in SOP form
13	2	Karnaugh map Minimization in POS form
14	2	Karnaugh map Minimization with Don't care conditions
15	2	Quine - McCluskey method of minimization without Don't care conditions
16	2	Quine - McCluskey method of minimization with Don't care conditions
17	3	**Digital Logic Gate Characteristics:** TTL logic gate characteristics.
18	3	Theory & operation of TTL NAND gate circuitry
19	3	Open collector TTL
20	3	Three state output logic
21	3	TTL subfamilies
22	3	MOS& CMOS logic families
23	3	Realization of logic gates in RTL,ECL,DTL
24	3	Realization of logic gates in C-MOS & MOSFET
25	4	**Combinational Circuits:** Combinational logic circuit design
26	4	Designing of adder, subtractor
27	4	Designing of BCD adder
28	4	Designing of encoder
29	4	Designing of decoder
30	4	Designing of BCD to 7-segment decoder
31	4	Designing of multiplexer
32	4	Designing of demultiplexer
33	5	**Sequential Circuits:** Latches, Flip-flops

34	5	SR, JK, D, T Flip Flop Characteristic table and equation
35	5	Master-Slave Characteristic table and equation
36	5	counters and their design, Asynchronous counters
37	5	Synchronous Up/Down counters
38	5	Programmable counters
39	5	State table and state transition diagram
40	5	sequential circuits design methodology. Registers –shift registers

TEXT/REFERENCE BOOKS

1. Modern Digital Electronics, R.P Jain, Tata McGraw-Hill Education
2. Digital Circuit & Logic Design, Morris Mano, Prentice Hall of India
3. Digital Principles & Applications, A.P.Malvino & D.P Leach, Tata McGraw-Hill Education

Teaching and Learning resources:

- **MOOC (NPTEL):** - https://onlinecourses.nptel.ac.in/noc19_ee51/preview

Assessment Methodology:

1. Viva and circuit design in practical lab.
2. Numerical Assignment
3. Two Midterm exams where student have to showcase subjective learning.
4. Final Exam (subjective paper) at the end of the semester.

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Roll No _____

3EU3023

B.Tech. III-Sem. (Main/Back) Exam Jan. 2019
Computer Science Engineering
3CSU03 Digital Electronics
3EU3023
(Common to CS/IT)

Time: 03 Hours
Min.Passing marks: 33

Maximum Marks: 100

Instructions to candidates: -

PART A : Short answer questions (up to 25 words) 10 x 2 marks = 20 marks. All ten questions are compulsory.

PART B : Analytical/Problem Solving questions (up to 100 words) 6 x 5 marks = 30 marks. Candidates have to answer six questions out of eight.

PART C : Descriptive/Analytical/Problem solving questions 5 x 10 marks = 50 marks. Candidates have to answer five questions out of seven

PART A

1. What are universal gates? Why are they called so?
2. Represent decimal number (127) in Excess-3, BCD and Gray code
3. Simplify: F= (AB'+A'B)' (A+B).
4. How many 2:1 Multiplexer will be required to realize 128:1 Multiplexer? What is the use of select line in MUX?
5. What is Race around condition?
6. Explain Half Adder circuit. Also give its circuit realization
7. Differentiate between synchronous and asynchronous counters.
8. Explain in short Universal shift register
9. What do you mean by prime implicants and essential prime implicants?

10. Differentiate between combinational circuits and sequential circuits.

PART B

1. Explain Master slave JK flip-flop in details.

2. Design a 3-bit synchronous Up/Down counters.

3. Implement a Full Subtracter using a 3 to 8 Decoder.

4. Realize the following Boolean function using 4:1 Multiplexer

$$F(A,B,C,D) = \Sigma m(0, 1, 2, 4, 6, 9, 12, 14)$$

5. Perform BCD Addition if A=0111, B=1000. Also, draw the circuit diagram for one digit BCD adder.

6. Draw the logic diagram of a 2-line to 4-line decoder/demultiplexer using two input NOR gate only.

7. Perform using 2's complement arithmetic: (a) 47-21 (b) 23-43 (c) 48-(-23)

8. Using K Map simplify the product-of-sum form the function given by

$F(A,B,C,D) = \Pi M(0, 6, 10, 12) + d(2,4,8,9,14,15)$ Realize it using logic gates.

PART C

1. Explain the process of flip-flop interconversion. Convert T-FF into JK flip-flop.

2. Simplify the logic function using Quine MacClusky minimization technique.

$$F(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13)$$

3. Construct a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use the conventional sequential circuit design procedure using JK FF.

4. Convert the following numbers as required in each case.

(a) $(123.45)_{10} = (?)_2$ (b) $(25.625)_{10} = (?)_{16}$ (c) $(603.23)_8 = (?)_2$

(d) $(ABCD)_{16} = (?)_2$ (e) $(15C.38)_{16} = (?)_8$

5. Explain BCD to 7-segment decoder.

6. Make a K-map for the function: $F=AB+AC'+C+AD+AB'C+ABC$., Express F in Canonical SOP form. Realize the minimized expression using NAND gate only.

7. Design: (a) BCD to excess-3 encoder (b) Binary to Gray decoder

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(Principal)

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B. TECH 2nd – YEAR (III SEM.) – MT-I

Digital Electronics (**3CS3-04**)

Time:2 Hr **Max. Marks: 70**

Note:

1) The paper is divided into 2 parts: Part-A & Part-B.
2) Part-A contains 10 questions and carries 2 marks each.
3) Part-B contains 5 questions. Each question is having two options and carries 10 marks each.

Part- A (20 Marks)

A. Explain in detail with example about fixed-point representation.	CO 1
B. Find the excess 3 equivalent of: 345 & Find 9's Compliment of: 1423	CO 1
C. Realize following expression using Universal NAND gate only $Y = AB + B'C$	CO 2
D. Design 8:1 MUX using basic gates.	CO 4
E. Design Half subtractor circuit with circuit diagram.	CO 4
F. Perform the following subtraction using 2's Compliment method. i) 11011 – 11001 ii) 11001 – 11011	CO 1
G. Convert the following numbers as required in each case $(603.23)_8 = (?)_2$ $(603.23)_8 = (?)_2$ $(15C.38)_{16} = (?)_8$	CO 1
H. Simplify the following Boolean expression $A[B+C(AB + AC)']$	CO 1
I. Express the function $Y = A + B'C$ • Canonical SOP form & Canonical POS form	CO 2
J. Simplify the expression using K-Map π (0,1,4,5,6,8,9,12,13,14)	CO 2

Part- B (40 Marks)

1. Explain in detail with example weighted binary codes.	CO1
OR	
1. Explain in detail with example non- weighted binary codes.	CO1

2. Reduce the following Boolean function using Quine Mc-Cluskey $Y = \sum_m (0,2,3,6,7) + \sum_d (8,10,11,15)$	CO 2
OR	
2. Design Full adder circuit and draw the circuit diagram for 4 bit ripple carry adder.	CO 4

3. Explain in detail about difference between Error detection and correction codes. Also explain in detail about Parity Codes & Hamming Code	CO1
OR	
3. Reduce the following Boolean function using Quine Mc-Cluskey $Y = \sum_m (1,3,4,5,9,10,11) + \sum_d (6,8)$	CO2

4. Design a BCD adder circuit using full adder IC 7483	CO 4
OR	
4. Design Decimal to BCD encoder	CO 4

5. Design BCD to Excess 3 Code converter	CO 4
OR	
5. Design 3 to 8 decoder circuit.	CO 4

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(Principal)

TECHNO INDIA NJR INSTITUTE OF TECHNOLOGY
B. TECH II – YEAR (III SEM.)
Computer Science & Engineering
Digital Electronic (3CS3-04)
Mid Term II

Max Marks: 70 **Time: 2 Hrs**

Note:
1) The paper is divided into 2 parts: Part-A and, Part-B
2) Part-A contains 10 questions and carries 2 mark each.
3) Part-B contains 5 questions. Each question is having two options and carries 10 marks each.

PART – A

1.	Design 16:1 Mux using 2:1 Mux only.	[CO4]
2.	Design 1:8 De-mux using basic gates.	[CO4]
3.	Realize D flip flop using JK flip flop.	[CO5]
4.	Draw circuit diagram of PISO shift register and explain.	[CO5]
5.	State the steps for sequential circuit design.	[CO5]
6.	Explain the working of JK flip flop.	[CO5]
7.	Define VIH, VIL, VOL, VOH.	[CO3]
8.	Write short note of RTL & DTL logic family.	[CO3]
9.	Draw CMOS circuit for AND gate.	[CO3]
10.	Draw AND gate using DTL logic.	[CO3]

PART – B

1.	Design a synchronous counter with the following binary sequence: 0, 4, 2 ,1 6 and repeat using JK flip flop	[CO5]
	OR	
1.	Explain Race Around Condition and working of Master slave JK flip flop.	[CO5]

2.	Design Mod-12 asynchronous up counter and draw the output waveforms.	[CO5]
	OR	
2.	Design 3-bit synchronous UP / Down counter	[CO5]

3.	Draw the circuit diagram of TTL NAND gate with totem pole output configuration and explain its working.	[CO3]
	OR	
3.	Draw the CMOS circuit diagram for a) NAND gate b) NOR Gate c) XOR gate	[CO3]

4.	Explain the following Digital IC characteristic parameters: a) Noise Margin b) Speed of operation c) Fan in & Fan Out	[CO3]
	OR	
4.	What are the different logic families, draw the tree and explain the classification	[CO3]

5.	Design BCD to Excess 3 encoder	[CO4]
	OR	
5.	Design Binary to Gray decoder	[CO4]

All the Best

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(Principal)

Assignment 2
Combinational logic circuits

Question 1:

A combinational circuit is defined by the following three Boolean functions:

F1(x,y,z)=x'y'z'+xz

F2(x,y,z)=xy'z'+x'y

F3(x,y,z)=x'y'z+xy

a. Design the combinational circuit that implements the functions.

b. Design the combinational circuit that implements the functions with a decoder and external gates.

Question 2:

A circuit implements the Boolean function **F (A,B,C,D)=A'B'C'D'+A'BCD'+AB'C'D'+ABC'D** It is found that the circuit input combinations **A'B'CD', A'BC'D', AB'CD'** can never occur.

a. Find a simpler expression for F using the proper "do not" care condition.

b. Design the circuit implementing the simplified expression of F using multilevel NAND.

Question 3:

Consider the function F with 3 inputs:

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Draw a circuit for F using only one 4-to-1 multiplexer and one NOT gates

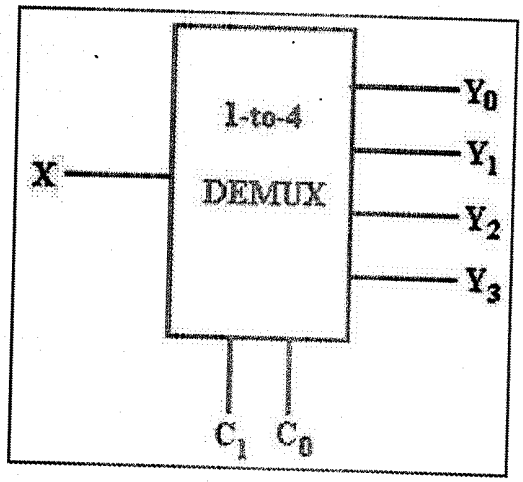
Question 4:

The De-multiplexer is the inverse of the multiplexer, in that it takes **one data input** and **n selection inputs**. It has **2^n outputs.** A 1to 4 De-multiplexer is represented by the following block diagram:

Depending on the diagram and the multiplexer implementation you have studied, build the following:

a. The Truth table for the given De-multiplexer.

b. The combinational logic circuit that builds the given De-multiplexer.



Miss. Dareen Hamoudeh

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(Principal)

Assignment 3

Part-A

1. What are universal gates? Why are they called so?
2. Represent decimal number (127) in Excess-3, BCD and Gray code
3. Simplify: F= (AB'+A'B)' (A+B).
4. How many 2:1 Multiplexer will be required to realize 128:1 Multiplexer? What is the use of select line in MUX?
5. What is Race around condition?
6. Explain Half Adder circuit. Also give its circuit realization
7. Differentiate between synchronous and asynchronous counters.
8. Explain in short Universal shift register
9. What do you mean by prime implicants and essential prime implicants?

Part-B

1. Explain Master slave JK flip-flop in details.
2. Design a 3-bit synchronous Up/Down counters.
3. Implement a Full Subtracter using a 3 to 8 Decoder.
4. Realize the following Boolean function using 4:1 Multiplexer

$$F(A,B,C,D) = \Sigma m(0, 1, 2, 4, 6, 9, 12, 14)$$

5. Perform BCD Addition if A=0111, B=1000 Also, draw the circuit diagram for one digit BCD adder.
6. Draw the logic diagram of a 2-line to 4-line decoder/demultiplexer using two input NOR gate only.
7. Perform using 2's complement arithmetic: (a) 47-21 (b) 23-43 (c) 48-(-23)
8. Using K Map simplify the product-of-sum form the function given by
   $F(A,B,C,D) = \Pi M(0, 6, 10, 12) + d(2,4,8,9,14,15)$ Realize it using logic gates.

Part-C

1. Explain the process of flip-flop interconversion. Convert T-FF into JK flip-flop.
2. Simplify the logic function using Quine MacClusky minimization technique.
$F(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13)$
3. Construct a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use the conventional sequential circuit design procedure using JK FF.
4. Convert the following numbers as required in each case.
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(d) $(ABCD)_{16} = (?)_2$ (e) $(15C.38)_{16} = (?)_8$
5. Explain BCD to 7-segment decoder.
6. Make a K-map for the function: $F=AB+AC'+C+AD+AB'C+ABC$. Express F in Canonical SOP form. Realize the minimized expression using NAND gate only.
7. Design: (a) BCD to excess-3 encoder (b) Binary to Gray decoder

Sample VIVA Questions

1. What is meant by radix (or base) of a number system?
2. What is weighted code? Give one example.
3. What is non-weighted code?
4. What is difference between LSB and MSB?
5. What is meant by BCD code?
6. What is excess-3 code?
7. Why hexadecimal code is widely used in digital system?
8. What is the difference between binary code and BCD?
9. Explain the use of excess-3 code.
10. What are the advantages of gray code?
11. What is an alphanumeric code?
12. What are the basic logic elements?
13. What is a truth table?
14. Define the positive logic and negative logic?
15. What is the specialty of NAND and NOR gates?
16. What is minterm ?
17. What is the difference between canonical form and standard form?
18. What is karnaugh map?
19. What is multiplexer & De-multiplexer?
20. What is Encoder & Decoder?
21. What is sequential circuits?
22. What is a flipflop?
23. What is difference between synchronous and asynchronous counters?
24. What is a ripple counter?
25. What are the Characteristics of Digital ICs?
26. Differentiate between Combinational Circuits and Sequential Circuits?
27. Differentiate between Synchronous and Asynchronous Counters?
28. Explain working of TTL NAND gate totempole configuration.
29. What is the advantage of using open collector output in TTL logic gates rather than using totem pole output?
30. What is the advantage of floating-point representation compared to fixed point representation?

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(Principal)

Digital Electronics MCQs [set-1]

1. Any number with an exponent of zero is equal to:

A. zero

B. one

C. that number

D. ten

Answer: B

---

2. In the decimal numbering system, what is the MSD?

A. the middle digit of a stream of numbers

B. the digit to the right of the decimal point

C. the last digit on the right

D. the digit with the most weight

Answer: D

---

3. Which of the following statements does NOT describe an advantage of digital technology?

A. the values may vary over a continuous range.

B. the circuits are less affected by noise.

C. the operation can be programmed.

D. information storage is easy.

Answer: A

---

4. The generic array logic (GAL) device is _____.

A. one-time programmable

B. reprogrammable

C. a cmos device

D. reprogrammable and a cmos device

Answer: B

5. The range of voltages between VL(max) and VH(min) are _____.

A. unknown

B. unnecessary

C. unacceptable

D. between 2 v and 5 v

Answer: C

6. What is a digital-to-analog converter?

A. it takes the digital information from an audio cd and converts it to a usable form.

B. it allows the use of cheaper analog techniques, which are always simpler.

C. it stores digital data on a hard drive.

D. it converts direct current to alternating current.

Answer: A

7. What are the symbols used to represent digits in the binary number system?

A. 0,1

B. 0,1,2

C. 0 through 8

D. 1,2

Answer: A

8. A full subtracter circuit requires _____.

A. two inputs and two outputs

B. two inputs and three outputs

C. three inputs and one output

D. three inputs and two outputs

Answer: D

---

9. The output of an AND gate is LOW _____.

A. all the time

B. when any input is low

C. when any input is high

D. when all inputs are high

Answer: B

---

10. Give the decimal value of binary 10010.

A. 610

B. 910

C. 1810

D. 2010

Answer: C

---

11. Parallel format means that:

A. each digital signal has its own conductor.

B. several digital signals are sent on each conductor.

C. both binary and hexadecimal can be used.

D. no clock is needed.

Answer: A

---

12. A decoder converts _____.

A. noncoded information into coded form

B. coded information into noncoded form

C. highs to lows

D. lows to highs

Answer: B

---

13. A DAC changes _____.

A. an analog signal into digital data

B. digital data into an analog signal

C. digital data into an amplified signal

D. none of the above

Answer: B

---

14. The output of a NOT gate is HIGH when _____.

A. the input is low

B. the input is high

C. the input changes from low to high

D. voltage is removed from the gate

Answer: A

---

15. The output of an OR gate is LOW when _____.

A. all inputs are low

B. any input is low

C. any input is high

D. all inputs are high

Answer: A

---

16. Which of the following is not an analog device?

A. thermocouple

B. current flow in a circuit

C. light switch

D. audio microphone

Answer: C

---

17. A demultiplexer has _____.

A. one data input and a number of selection inputs, and they have several outputs

B. one input and one output

C. several inputs and several outputs

D. several inputs and one output

Answer: A

---

18. A flip-flop has _____.

A. one stable state

B. no stable states

C. two stable states

D. none of the above

Answer: C

---

19. Digital signals transmitted on a single conductor (and a ground) must be transmitted in:

A. slow speed.

B. parallel.

C. analog.

D. serial.

Answer: D

20. In a certain digital waveform, the period is four times the pulse width. The duty cycle is _____.

A. 0%

B. 25%

C. 50%

D. 100%

Answer: B

21. Select the statement that best describes the parity method of error detection:

A. parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.

B. parity checking is not suitable for detecting single-bit errors in transmitted codes.

C. parity checking is best suited for detecting single-bit errors in transmitted codes.

D. parity checking is capable of detecting and correcting errors in transmitted codes.

Answer: C

22. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):

A. ex-nor gate

B. or gate

C. ex-or gate

D. nand gate

Answer: A

23. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

A. ex-nor gate

B. or gate

C. ex-or gate

D. nand gate

Answer: C

---

24. Identify the type of gate below from the equation

A. ex-nor gate

B. or gate

C. ex-or gate

D. nand gate

Answer: C

---

25. Parity systems are defined as either_____ or _____ and will add an extra _____ tothe digital information being transmitted.

A. positive, negative, byte

B. odd, even, bit

C. upper, lower, digit

D. on, off, decimal

Answer: B

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Digital Electronics MCQs [set-4]

76. Convert 59.7210 to BCD.

A. 111011

B. 01011001.01110010

C. 1110.11

D. 0101100101110010

Answer: B

---

77. Convert 8B3F16 to binary.

A. 35647

B. 011010

C. 1011001111100011

D. 1000101100111111

Answer: D

---

78. Which is typically the longest: bit, byte, nibble, word?

A. bit

B. byte

C. nibble

D. word

Answer: D

---

79. Assign the proper odd parity bit to the code 111001.

A. 1111011

B. 1111001

C. 0111111

D. 0011111

Answer: B

---

80. Convert decimal 64 to binary.

A. 01010010

B. 01000000

C. 00110110

D. 01001000

Answer: B

---

81. Convert hexadecimal value C1 to binary.

A. 11000001

B. 1000111

C. 111000100

D. 111000001

Answer: A

---

82. The given hexadecimal number (1E.53)16 is equivalent to

A. (35.684)8

B. (36.246)8

C. (34.340)8

D. (35.599)8

Answer: B

---

83. The octal number (651.124)8 is equivalent to

A. 16

B. (1b0.10)16

C. (1a8.a3)16

D. (1b0.b0)16

Answer: A

---

84. The octal equivalent of the decimal number (417)10 is

A. (641)8

B. (619)8

C. (640)8

D. (598)8

Answer: A

---

85. Convert the hexadecimal number (1E2)16 to decimal:

A. 480

B. 483

C. 482

D. 484

Answer: C

---

86. (170)10 is equivalent to

A. (fd)16

B. (df)16

C. (aa)16

D. (af)16

Answer: C

---

87. Convert the binary number (01011.1011)2 into decimal:

A. (11.6875)10

B. (11.5874)10

C. (10.9876)10

D. (10.7893)10

Answer: A

---

88. 1011)2 = (11.6875)10

A. (111101)2

B. (010100)2

C. (111100)2

D. (101010)2

Answer: B

---

89. On addition of +38 and -20 using 2's complement, we get

A. 11110001

B. 100001110

C. 010010

D. 110101011

Answer: C

---

90. On addition of -46 and +28 using 2's complement, we get

A. 00101110

B. 0101110

C. 00101111

D. 1001111

Answer: B

---

91. On subtracting +28 from +29 using 2's complement, we get

A. 11111010

B. 111111001

C. 100001

D. 1

Answer: D

---

92. The decimal number 10 is represented in its BCD form as

A. 10100000

B. 01010111

C. 00010000

D. 00101011

Answer: C

---

93. When numbers, letters or words are represented by a special group of symbols, this process is called

A. decoding

B. encoding

C. digitizing

D. inverting

Answer: B

---

94. Carry out BCD subtraction for (68) – (61) using 10's complement method.

A. 00000111

B. 01110000

C. 100000111

D. 011111000

Answer: A

95. How many bits would be required to encode decimal numbers 0 to 9999 in straight binary codes?

A. 12

B. 14

C. 16

D. 18

Answer: B

96. The decimal equivalent of the excess-3 number 110010100011.01110101 is

A. 970.42

B. 1253.75

C. 861.75

D. 1132.87

Answer: A

97. In boolean algebra, the OR operation is performed by which properties?

A. associative properties

B. commutative properties

C. distributive properties

D. all of the mentioned

Answer: D

98. The expression for Absorption law is given by

A. a + ab = a

B. a + ab = b

C. ab + aa' = a

D. a + b = b + a

Answer: A

---

99. According to boolean law: A + 1 = ?

A. 1

B. a

C. 0

D. a'

Answer: A

---

100. The involution of A is equal to

A. a

B. a'

C. 1

D. 0

Answer: A

Digital Electronics MCQs [set-5]

101. DeMorgan's theorem states that

A. (ab)' = a' + b'

B. (a + b)' = a' * b

C. a' + b' = a'b'

D. (ab)' = a' + b

Answer: A

102. (A + B)(A' * B') = ?

A. 1

B. 0

C. ab

D. ab'

Answer: B

103. Complement of the expression A'B + CD' is

A. (a' + b)(c' + d)

B. (a + b')(c' + d)

C. (a' + b)(c' + d)

D. (a + b')(c + d')

Answer: B

104. Simplify Y = AB' + (A' + B)C.

A. ab' + c

B. ab + ac

C. a'b + ac'

D. ab + a

Answer: A

---

105. The boolean function A + BC is a reduced form of

A. ab + bc

B. (a + b)(a + c)

C. a'b + ab'c

D. (a + c)b

Answer: B

---

106. A is a circuit with only one output but can have multiple inputs.

A. logic gate

B. truth table

C. binary circuit

D. boolean circuit

Answer: A

---

107. There are 5 universal gates.

A. true

B. false

Answer: B

---

108. The Output is LOW if any one of the inputs is HIGH in case of a gate.

A. nor

B. nand

C. or

D. and

Answer: B

---

109. The complement of the input given is obtained in case of:

A. nor

B. and+nor

C. not

D. ex-or

Answer: C

---

110. How many AND gates are required to realize the following expression Y=AB+BC?

A. 4

B. 8

C. 1

D. 2

Answer: D

---

111. Number of outputs in a half adder

A. 1

B. 2

C. 3

D. 0

Answer: B

---

112. The gate is an OR gate followed by a NOT gate.

A. nand

B. exor

C. nor

D. exnor

Answer: C

---

113. The expression of a NAND gate is

A. a.b

B. a'b+ab'

C. (a.b)'

D. (a+b)'

Answer: C

---

114. Which of the following correctly describes the distributive law.

A. (a+b)(c+d)=ab+cd

B. (a+b).c=ac+bc

C. (ab)(a+b)=ab

D. (a.b)c=ac.ab

Answer: B

---

115. The logical sum of two or more logical product terms is called

A. sop

B. pos

C. or operation

D. nand operation

Answer: A

---

116. The expression Y=(A+B)(B+C)(C+A) shows the operation.

A. and

B. pos

C. sop

D. nand

Answer: B

---

117. The canonical sum of product form of the function y(A,B) = A + B is

A. ab + bb + a'a

B. ab + ab' + a'b

C. ba + ba' + a'b'

D. ab' + a'b + a'b'

Answer: B

---

118. A variable on its own or in its complemented form is known as a

A. product term

B. literal

C. sum term

D. word

Answer: B

---

119. Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented.

A. terms

B. words

C. numbers

D. nibble

Answer: A

---

120. Canonical form is a unique way of representing

A. sop

B. minterm

C. boolean expressions

D. pos

Answer: C

---

121. There are Minterms for 3 variables (a, b, c).

A. 0

B. 2

C. 8

D. 1

Answer: C

---

122. expressions can be implemented using either (1) 2-level AND- OR logic circuits or (2) 2-level NAND logic circuits.

A. pos

B. literals

C. sop

D. pos

Answer: C

---

123. There are cells in a 4-variable K- map.

A. 12

B. 16

C. 18

D. 8

Answer: B

124. The prime implicant which has at least one element that is not present in any other implicant is known as

A. essential prime implicant

B. implicant

C. complement

D. prime complement

Answer: A

125. Product-of-Sums expressions can be implemented using

A. 2-level or-and logic circuits

B. 2-level nor logic circuits

C. 2-level xor logic circuits

D. both 2-level or-and and nor logic circuits

Answer: D

Digital Electronics MCQs [set-6]

126. Each product term of a group, w'.x.y' and w.y, represents the in that group.

A. input

B. pos

C. sum-of-minterms

D. sum of maxterms

Answer: C

---

127. It should be kept in mind that don't care terms should be used along with the terms that are present in

A. minterms

B. expressions

C. k-map

D. latches

Answer: A

---

128. Using the transformation method you can realize any POS realization of OR-AND with only.

A. xor

B. nand

C. and

D. nor

Answer: D

---

129. In case of XOR/XNOR simplification we have to look for the following

A. diagonal adjacencies

B. offset adjacencies

C. straight adjacencies

D. both diagonal and offset adjencies

Answer: D

130. In which of the following gates the output is 1 if and only if at least one input is 1?

A. and

B. nor

C. nand

D. or

Answer: D

131. The time required for a gate or inverter to change its state is called

A. rise time

B. decay time

C. propagation time

D. charging time

Answer: C

132. Odd parity of word can be conveniently tested by

A. or gate

B. and gate

C. nand gate

D. xor gate

Answer: D

133. The number of full and half adders are required to add 16-bit number is

A. 8 half adders, 8 full adders

B. 1 half adders, 15 full adders

C. 16 half adders, 0 full adders

D. 4 half adders, 12 full adders

Answer: B

---

134. An OR gate can be imagined as

A. switches connected in series

B. switches connected in parallel

C. mos transistor connected in series

D. bjt transistor connected in series

Answer: B

---

135. In parts of the processor, adders are used to calculate

A. addresses

B. table indices

C. increment and decrement operators

D. all of the mentioned

Answer: D

---

136. How many full adders are required to construct an m-bit parallel adder?

A. m/2

B. m

C. m-1

D. m+1

Answer: C

---

137. In which operation carry is obtained?

A. subtraction

B. addition

C. multiplication

D. both addition and subtraction

Answer: B

---

138. If A and B are the inputs of a half adder, the sum is given by

A. a and b

B. a or b

C. a xor b

D. a ex-nor b

Answer: C

---

139. If A and B are the inputs of a half adder, the carry is given by

A. a and b

B. a or b

C. a xor b

D. a ex-nor b

Answer: A

---

140. Half-adders have a major limitation in that they cannot

A. accept a carry bit from a present stage

B. accept a carry bit from a next stage

C. accept a carry bit from a previous stage

D. accept a carry bit from the following stages

Answer: C

---

141. The difference between half adder and full adder is

A. half adder has two inputs while full adder has four inputs

B. half adder has one output while full adder has two outputs

C. half adder has two inputs while full adder has three inputs

D. all of the mentioned

Answer: C

---

142. If A, B and C are the inputs of a full adder then the sum is given by

A. a and b and c

B. a or b and c

C. a xor b xor c

D. a or b or c

Answer: C

---

143. If A, B and C are the inputs of a full adder then the carry is given by

A. a and b or (a or b) and c

B. a or b or (a and b) c

C. (a and b) or (a and b)c

D. a xor b xor (a xor b) and c

Answer: A

---

144. How many AND, OR and EXOR gates are required for the

configuration of full

A. 1, 2, 2

B. 2, 1, 2

C. 3, 1, 2

D. 4, 0, 1

Answer: B

---

145. Half subtractor is used to perform subtraction of

A. 2 bits

B. 3 bits

C. 4 bits

D. 5 bits

Answer: A

---

146. How many outputs are required for the implementation of a subtractor?

A. 1

B. 2

C. 3

D. 4

Answer: B

---

147. Let the input of a subtractor is A and B then what the output will be if A = B?

A. 0

B. 1

C. a

D. b

Answer: A

148. Let A and B is the input of a subtractor then the output will be

A. a xor b

B. a and b

C. a or b

D. a exnor b

Answer: A

149. Let A and B is the input of a subtractor then the borrow will be

A. a and b'

B. a' and b

C. a or b

D. a and b

Answer: B

150. What does minuend and subtrahend denotes in a subtractor?

A. their corresponding bits of input

B. its outputs

C. its inputs

D. borrow bits

Answer: C

Digital Electronics MCQs [set-7]

151. Full subtractor is used to perform subtraction of

A. 2 bits

B. 3 bits

C. 4 bits

D. 8 bits

Answer: B

152. The output of a full subtractor is same as

A. half adder

B. full adder

C. half subtractor

D. decoder

Answer: B

153. The full subtractor can be implemented using

A. two xor and an or gates

B. two half subtractors and an or gate

C. two multiplexers and an and gate

D. two comparators and an and gate

Answer: B

154. Why XOR gate is called an inverter?

A. because of the same input

B. because of the same output

C. it behaves like a not gate

D. it behaves like a and gate

Answer: C

---

155. Controlled buffers can be useful

A. to control the circuit's output into the bus

B. in comparison of component's output with its input

C. in increasing the output from its low input

D. all of the mentioned

Answer: A

---

156. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is

A. ex-nor gate

B. or gate

C. ex-or gate

D. nand gate

Answer: A

---

157. What is the first thing you will need if you are going to use a macro-function?

A. a complicated design project

B. an experienced design engineer

C. good documentation

D. experience in hdl

Answer: D

---

158. What is the major difference between half- adders and full-adders?

A. full-adders are made up of two half-adders

B. full adders can handle double-digit numbers

C. full adders have a carry input capability

D. half adders can handle only single-digit numbers

Answer: C

159. The binary subtraction of 0 – 0 = ?

A. difference = 0, borrow = 0

B. difference = 1, borrow = 0

C. difference = 1, borrow = 1

D. difference = 0, borrow = 1

Answer: A

160. How many basic binary subtraction operations are possible?

A. 1

B. 4

C. 3

D. 2

Answer: B

161. When performing subtraction by addition in the 2's-complement system

A. the minuend and the subtrahend are both changed to the 2's-complement

B. the minuend is changed to 2's- complement and the subtrahend is left in its original form

C. the minuend is left in its original form and the subtrahend is changed to its 2's- complement

D. the minuend and subtrahend are both left in their original form

Answer: C

162. What are the two types of basic adder circuits?

A. sum and carry

B. half-adder and full-adder

C. asynchronous and synchronous

D. one and two's-complement

Answer: B

---

163. Which of the following is correct for full adders?

A. full adders have the capability of directly adding decimal numbers

B. full adders are used to make half adders

C. full adders are limited to two inputs since there are only two binary digits

D. in a parallel full adder, the first stage may be a half adder

Answer: D

---

164. The selector inputs to an arithmetic/logic unit (ALU) determine the

A. selection of the ic

B. arithmetic or logic function

C. data word selection

D. clock frequency to be used

Answer: B

---

165. The inverter can be produced with how many NAND gates?

A. 2

B. 1

C. 3

D. 4

Answer: B

166. What are carry generate combinations?

A. if all the input are same then a carry is generated

B. if all of the output are independent of the inputs

C. if all of the input are dependent on the output

D. if all of the output are dependent on the input

Answer: B

167. How many shift registers are used in a 4 bit serial adder?

A. 4

B. 3

C. 2

D. 5

Answer: C

168. A D flip-flop is used in a 4-bit serial adder, why?

A. it is used to invert the input of the full adder

B. it is used to store the output of the full adder

C. it is used to store the carry output of the full adder

D. it is used to store the sum output of the full adder

Answer: C

169. What is ripple carry adder?

A. the carry output of the lower order stage is connected to the carry input of the next higher order stage

B. the carry input of the lower order stage is connected to the carry output of the next higher order stage

C. the carry output of the higher order stage is connected to the carry input of the next lower order stage

D. the carry input of the higher order stage is connected to the carry output of the lower order stage

Answer: A

---

170. If minuend = 0, subtrahend = 1 and borrow input = 1 in a full subtractor then the borrow output will be

A. 0

B. 1

C. floating

D. high impedance

Answer: B

---

171. The decimal number system represents the decimal number in the form of

A. hexadecimal

B. binary coded

C. octal

D. decimal

Answer: B

---

172. 29 input circuit will have total of

A. 32 entries

B. 128 entries

C. 256 entries

D. 512 entries

Answer: D

---

173. BCD adder can be constructed with 3 IC packages each of

A. 2 bits

B. 3 bits

C. 4 bits

D. 5 bits

Answer: C

---

174. The output sum of two decimal digits can be represented in

A. gray code

B. excess-3

C. bcd

D. hexadecimal

Answer: C

---

175. The addition of two decimal digits in BCD can be done through

A. bcd adder

B. full adder

C. ripple carry adder

D. carry look ahead

Answer: A

Digital Electronics MCQs [set-8]

176. 3 bits full adder contains

A. 3 combinational inputs

B. 4 combinational inputs

C. 6 combinational inputs

D. 8 combinational inputs

Answer: D

---

177. The simplified expression of full adder carry is

A. c = xy+xz+yz

B. c = xy+xz

C. c = xy+yz

D. c = x+y+z

Answer: A

---

178. Complement of F' gives back

A. f'

B. f

C. ff

D. ff'

Answer: B

---

179. Decimal digit in BCD can be represented by

A. 1 input line

B. 2 input lines

C. 3 input lines

D. 4 input lines

Answer: D

---

180. The number of logic gates and the way of their interconnections can be classified as

A. logical network

B. system network

C. circuit network

D. gate network

Answer: A

---

181. What is a multiplexer?

A. it is a type of decoder which decodes several inputs and gives one output

B. a multiplexer is a device which converts many signals into one

C. it takes one input and results into many output

D. it is a type of encoder which decodes several inputs and gives one output

Answer: B

---

182. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

A. data selector

B. data distributor

C. both data selector and data distributor

D. demultiplexer

Answer: A

---

183. It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large

number of

A. inputs

B. outputs

C. selection lines

D. enable lines

Answer: A

---

184. Which is the major functioning responsibility of the multiplexing combinational circuit?

A. decoding the binary information

B. generation of all minterms in an output function with or-gate

C. generation of selected path between multiple sources and a single destination

D. encoding of binary information

Answer: C

---

185. 6 MULTIPLEXER

A. to apply vcc

B. to connect ground

C. to active the entire chip

D. to active one half of the chip

Answer: C

---

186. One multiplexer can take the place of

A. several ssi logic gates

B. combinational logic circuits

C. several ex-nor gates

D. several ssi logic gates or combinational logic circuits

Answer: D

---

187. A digital multiplexer is a combinational circuit that selects

A. one digital information from several sources and transmits the selected one

B. many digital information and convert them into one

C. many decimal inputs and transmits the selected information

D. many decimal outputs and accepts the selected information

Answer: A

---

188. If the number of n selected input lines is equal to 2^m then it requires select lines.

A. 2

B. m

C. n

D. 2n

Answer: B

---

189. How many select lines would be required for an 8-line-to-1-line multiplexer?

A. 2

B. 4

C. 8

D. 3

Answer: D

---

190. A basic multiplexer principle can be demonstrated through the use of a

A. single-pole relay

B. dpdt switch

C. rotary switch

D. linear stepper

Answer: C

---

191. How many NOT gates are required for the construction of a 4-to-1 multiplexer?

A. 3

B. 4

C. 2

D. 5

Answer: C

---

192. In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is

A. x0

B. x1

C. x2

D. x3

Answer: B

---

193. The enable input is also known as

A. select input

B. decoded input

C. strobe

D. sink

Answer: C

---

194. The word demultiplex means

A. one into many

B. many into one

C. distributor

D. one into many as well as distributor

Answer: D

---

195. Why is a demultiplexer called a data distributor?

A. the input will be distributed to one of the outputs

B. one of the inputs will be selected for the output

C. the output will be distributed to one of the inputs

D. single input to single output

Answer: A

---

196. Most demultiplexers facilitate which type of conversion?

A. decimal-to-hexadecimal

B. single input, multiple outputs

C. ac to dc

D. odd parity to even parity

Answer: B

---

197. In 1-to-4 demultiplexer, how many select lines are required?

A. 2

B. 3

C. 4

D. 5

Answer: A

---

198. In a multiplexer the output depends on its

A. data inputs

B. select inputs

C. select outputs

D. enable pin

Answer: B

---

199. In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be

A. y0

B. y1

C. y2

D. y3

Answer: B

---

200. In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be

A. y0

B. y1

C. y2

D. y3

Answer: D

For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
(Principal)