# Techno India NJR Institute of Technology

# Course File

# Session 2020-21

# Digital System Design (3EC4-04)

Pradeep Chhawchharia
( Professor)
**Department of ECE**

For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
(Principal)

# RAJASTHAN TECHNICAL UNIVERSITY, KOTA

**SYLLABUS**

**II Year - III Semester: B.Tech. (Electronics & Communication Engineering)**

## 3EC4-04: Digital System Design

**3 Credits** | **Max. Marks: 150 (IA:30, ETE:120)**

**3L:0T:0P** | **End Term Exam: 3 Hours**

| SN | Contents | Hours |
|---|---|---|
| 1 | Logic Simplification and Combinational Logic Design: Review of Boolean Algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh maps up to 6 variables, Binary codes, Code Conversion. | 7 |
| 2 | MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU | 8 |
| 3 | Sequential Logic Design: Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of Synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation. | 9 |
| 4 | Logic Families and Semiconductor Memories: TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS families and their interfacing, memory elements, Concept of Programmable logic devices like FPGA. Logic implementation using programmable devices. | 8 |
| 5 | VLSI Design flow: Design entry: Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits. | 8 |
| | **Total** | **40** |

## Course Overview:

## Course Outcomes:

| CO.NO. | Cognitive Level | Course Outcome |
|---|---|---|
| 1 | Comprehension | Develop the understanding of number system and its application in digital electronics. |
| 2 | Analysis | Development and analysis of K-map to solve the Boolean function to the simplest form for the implementation of compact digital circuits. |
| 3 | Synthesis | Design various combinational and sequential circuits using various metrics: switching speed, throughput/latency, gate count and area, energy dissipation and power. |
| 4 | Synthesis | Understanding Interfacing between digital circuits and analog component using Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) etc. |
| 5 | synthesis | Design and implement semiconductor memories, programmable logic devices (PLDs) and field programmable gate arrays (FPGA) in digital electronics. |

## Prerequisites:

1. Fundamentals of Boolean logics

## Course Outcome Mapping with Program Outcome:

| Course Outcome | Program Outcomes (PO's) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO. NO. | Domain Specific | | | | | Domain Independent | | | | | | |
| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
| CO1 | 3 | 2 | 2 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO2 | 3 | 2 | 3 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO3 | 2 | 2 | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO4 | 3 | 2 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO5 | 2 | 1 | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High) | | | | | | | | | | | | |

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## Course Coverage Module Wise:

| Lecture No. | Unit | Topic |
|---|---|---|
| 1 | **1** | **INTRODUCTION: OBJECTIVE, SCOPE AND OUTCOME OF THE COURSE.** |
| 2 | 1 | Review of Boolean Algebra |
| 3 | 1 | DeMorgan's Theorem, SOP & POS forms |
| 4 | 1 | Problem of SOP and POS forms of boolean functions |
| 5 | 1 | Simplification of karnaugh map up to 6 variables |
| 6 | 1 | Simplification of karnaugh map up to 6 variables |
| 7 | 1 | Simplification of karnaugh map up to 6 variables |
| 8 | **2** | **BINARY CODES AND CODE CONVERSION** |
| 9 | 2 | Binary codes and code conversion |
| 10 | 2 | Encoder, Decoder |
| 11 | 2 | Half and Full Adders, Subtractors, Serial and Parallel Adders |
| 12 | 2 | BCD Adder, Barrel shifter |
| 13 | 2 | S-R FF, edge triggered and level triggered |
| 14 | 2 | D and J-K FF |
| 15 | 2 | Master-Slave JK FF and T FF |
| 16 | **3** | **RIPPLE AND SYNCHRONOUS COUNTERS** |
| 17 | 3 | Other type of counters |
| 18 | 3 | Shift registers, Finite state machines, Asynchronous FSM |
| 19 | 3 | Design of synchronous FSM |
| 20 | 3 | Design of synchronous FSM |
| 21 | 3 | Design of synchronous FSM |
| 22 | 3 | Designing synchronous circuits (pulse train generator, pseudorandom binary sequence generator, clock generation) |
| 23 | 3 | TTL NAND gate, specifications, noise margin, propagation delay,fan-in, fan-out |
| 24 | 3 | TTL NAND gate |
| 25 | **4** | **TRISTATE TTL, ECL** |
| 26 | 4 | CMOS families and their interfacing |
| 27 | 4 | CMOS families and their interfacing |
| 28 | 4 | Read-Only Memory, Random Access Memory |
| 29 | 4 | Programmable Logic Arrays (PLA) |
| 30 | 4 | Programmable Array Logic (PAL) |
| 31 | 4 | Field Programmable Gate Array (FPGA) |
| 32 | 4 | Combinational PLD-Based State Machines |
| 33 | **5** | **STATE MACHINES ON A CHIP** |
| 34 | 5 | Schematic, FSM & HDL |
| 35 | 5 | Different modeling styles in VHDL |
| 36 | 5 | Data types and objects, Data flow |

| | | |
|---|---|---|
| 37 | 5 | Behavioral and Structural Modeling |
| 38 | 5 | Behavioral and Structural Modeling |
| 39 | 5 | Simulation VHDL constructs and codes for combinational andsequential circuits |
| 40 | 5 | Simulation VHDL constructs and codes for combinational andsequential circuits |

**TEXT/REFERENCE BOOKS**


1. Digital Circuit & Logic Design, Morris Mano, Prentice Hall of India.
2. Digital Principles & Applications, A.P. Malvino& D.P. Leach, Tata Mc-graw Hill, Delhi.


## Teaching and Learning resources:

### MOOC (NPTEL): -

## Assessment Methodology:

3. Viva and circuit design in practical lab.
4. Numerical Assignment
5. Two Midterm exams where student have to showcase subjective learning.
6. Final Exam (subjective paper) at the end of the semester.

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Roll No. Total No of Pages: 3

# 3E1147

## B. Tech. III - Sem. (Main / Back) Exam., Dec. 2019
## PCC Electronics & Communication Engineering
## 3EC4-04 Digital System Design
## Common For EC, EI

**Time: 3 Hours** **Maximum Marks: 120**

*Instructions to Candidates:*

***Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.***

*Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

1. NIL 2. NIL

## PART – A

**(Answer should be given up to 25 words only)** **[10×2=20]**

**All questions are compulsory**

Q.1 Find value of x for following equation:

$(135)_x + (531)_x = (666)_x$

Q.2 Convert $(1011)_{\text{gray code}}$ to excess-3 code.

Q.3 Find the sum of $(1.98)_{10} + (4.86)_{16}$.

Q.4 State the difference between flip flop and latch.

Q.5 Write the excitation table of RS flip flop.

Q.6 Define figure of merit for logic family.

Q.7 How many Boolean functions can be made from 3 variables?

Q.8 Write a VHDL code for $y=\overline{A}\overline{B}$ in structural style of modelling.

Q.9 How many flip flops are required to design modules 20 counter?

Q.10 If the present output of 4 – bit twisted ring counter is 1011, then find its output after 6 clock cycles.

## PART – B

**(Analytical/Problem solving questions)** **[5×8=40]**

**Attempt any five questions**

Q.1 How Ex-OR gate is used in parity bit generation and error detection at transmitter and receiver respectively? Explain using an example of 8-bit data.

Q.2 Convert following canonical form into standard form using tabulation method

$$Y=\sum m\,(4,5,6,11,13)+d\sum(0,2)$$

Q.3 Explain the procedure for conversion of RS flip flop into JK flip flop.

Q.4 Write the help of neat circuit diagram explain the interfacing of various logic families.

Q.5 Implement the following Boolean functions: http://www.rtuonline.com

(i) $Y=\overline{AB+CD}$ using CMOS

(ii) $Y = AB+C$ using PMOS

Q.6 Write a VHDL code for full adder in structural style of modelling.

Q.7 What is FSM? State the difference between Mealy and Moore state machines.

## PART – C

**(Descriptive/Analytical/Problem Solving/Design Questions)** **[4×15=60]**

**Attempt any four questions**

Q.1 (a) What are prime, essential and redundant implicants? Explain with an example.

(b) Signals A, B, C, D and $\overline{A}$ are available. Using only 8:1 mux and no other gate, implement the expression $F(A, B, C, D) = B\overline{C} + AB\overline{D} + \overline{A}\,\overline{C}D$

Q.2 The state diagram of a FSM is given below (Fig 1).

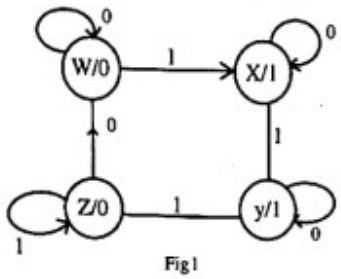


Fig 1

Show its state table, state assignment table and final implemented logic.

Q.3 Design a synchronous counter using JK flip flop to generate following sequence

0,7,5,3,2,1

Also write its state table, state assignment table and final implemented logic.

Q.4 (a) Design the 4-input priority encoder with truth table and draw its logic diagram.

(b) Draw and explain the logic diagram of BCD adder using two 4 bit adders and a correction detection circuit.

Q.5 Write a short note on following :

(i) FPGA

(ii) PLA

(iii) CPLD

(iv) PAL

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**B. Tech. III - Sem. (Main) Exam., Dec. - 2018**
**PCC Electronics & Communication Engineering**
**3EC4 – 04 Digital System Design**
**EC, EI**

**Time: 3 Hours** **Maximum Marks: 120**

*Instructions to Candidates:*

***Attempt all ten questions from Part A, selecting five questions from Part B and four questions from Part C.***

*Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

1. NIL

2. NIL

## PART – A

**(Answer should be given up to 25 words only)** **[10×2=20]**

**All questions are compulsory**

Q.1 Write Decimal no. $(125)_{10}$ in BCD.

Q.2 Convert $y = AB + \overline{A}\,\overline{B}$ (sop) form in equivalent POS form. [2]

Q.3 Define Fan-out of logic system. [2]

Q.4 Write the name of two modeling style in VHDL. [2]

Q.5 Draw the state diagram of any one finite state machine (FSM). [2]

Q.6 Find the total no. of select line, when a 8×1 Mux is implemented using 2×1 Mux. [2]

Q.7 Draw the circuit diagram of any two Dynamic memory cell. [2]

Q.8 Write any one use of tristate logic. [2]

Q.9 Write the name of one Parallel Adder. [2]

Q.10 Write VHDL code for $y = A\overline{B}$ in structural model. [2]

## PART – B

**(Analytical/Problem solving questions)** **[5×8=40]**

**Attempt any five questions**

Q.1 Derive a minimum cost circuit that implement the function- [8]

$$f(x_1 \ldots x_u) = \sum m(4,7,8,11) + D(12,15)$$

Q.2 Draw the output waveform of a four bit serial in parallel out shift register for six clocks. Assume the Data input is =10111011... [8]

Q.3 Implement y= A + BC in ECL logic and explain its working. [8]

Q.4 How SR FF is converted to JK FF? Draw its circuit diagram and explain. How the JK FF determine output when both J = K = 1? [8]

Q.5 Write VHDL code for a Half Adder in Data flow style. [8]

Q.6 How Mux is used for implement combinational logic? Implement y = A+BCD using a Mux. http://www.rtuonline.com [8]

Q.7 Draw the general diagram of a single bit serial Adder. Calculate the total delay taken in Addition of two four bit data in it. [8]

## PART – C

**(Descriptive/Analytical/Problem Solving/Design Question)** **[4×15=60]**

**Attempt any four questions**

Q.1 Draw the 2 input NAND gate using TTL logic and calculate its minimum noise level at input that disturb the true output for A = B = 0. Assume the supply is $V_{DD}$ = 9 volt. [15]

Q.2 The state diagram of a FSM is given below, design its logic (fig-2(c)) [15]

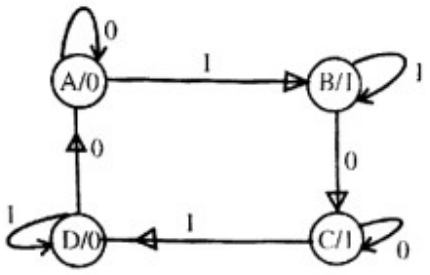


fig - 2(c)

Show its state table, state assignment table and final implemented logic.

Q.3 Draw the state diagram for the logic circuit shown in fig 3(c). [15]

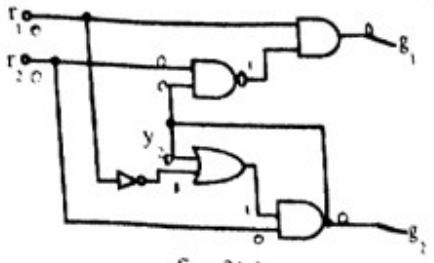


fig - 3(c)

Q.4 Design a 4 bit synchronous down counter using D-FF. Draw its state diagram and all design tables. [15]

Q.5 How FPGA are used for logic implement? Show the OR and AND Space for a 2 variable input. Also show the connection in FPGA for implement $y = \bar{A}\,\bar{B}$ in it. [15]

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