Techno India NJR Institute of Technology

Course File

Computer Architecture (5EC3-01)

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For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
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RAJASTHAN TECHNICAL UNIVERSITY, KOTA

SYLLABUS

III Year - V Semester: B.Tech. (Electronics & Communication Engineering)

5EC3-01: Computer Architecture

Credit: 2
2L+0T+0P

Max. Marks: 100(IA:20, ETE:80)
End Term Exam: 2 Hours

SN	Contents	Hours
1	Introduction: Objective, scope and outcome of the course.	1
2	Basic Structure of Computers, Functional units, software, performance issues software, machineinstructions and programs, Types of instructions, Instruction sets: Instruction formats, Assembly language, Stacks, Ques, Subroutines.	6
3	Processor organization, Information representation, number formats. Multiplication & division, ALU design, Floating Point arithmetic, IEEE 754 floating pointformats	5
4	Control Design, Instruction sequencing, Interpretation, Hard wired controlDesignmethods, and CPU control unit. Microprogrammed Control - Basic concepts, minimizing microinstruction size, multiplier control unit. Microprogrammed computers - CPU control unit	6
5	Memory organizations, device characteristics, RAM, ROM, Memory management, Concept ofCache & associative memories, Virtual memory.	5
6	System organization, Input - Output systems, Interrupt, DMA, Standard I/O interfacesConcept of parallel processing, Pipelining, Forms of parallel processing, interconnect network	5
	Total	28

Course Overview:

To study concepts related to Computer Data Representation, Micro-operations, Instructions, Programming the basic computer, Central Processing Unit, Computer Arithmetic, Memory Organization, Multiprocessors etc. which is vital to excel in the field of Computer Architecture domain.

Course Outcomes:

CO.NO.	Cognitive Level	Course Outcome
1	**Comprehension**	Develop an ability to understand the design and interconnection of various parts of a computer
2	**Application**	Develop an ability to understand and apply the basic computer arithmetic operations
3	**Synthesis**	Design & Develop interfacing circuitry an ability memories and input/output organization to CPU.

Prerequisites:

1. Fundamentals knowledge of Binary Number System.
2. Fundamentals knowledge of Combinational Circuit.
3. Fundamentals knowledge of Sequential circuit.

Course Outcome Mapping with Program Outcome:

Course Outcome	Program Outcomes (PO's)											
CO. NO.	Domain Specific					Domain Independent						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	1	0	0	0	0	0	0	0	0	0
CO2	3	3	2	0	0	0	0	0	0	0	0	0
CO3	2	1	2	2	2	0	0	0	0	0	0	0
1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High)												

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Course Coverage Module Wise:

Lecture No.	Unit	Topic
1	**1**	**INTRODUCTION: COMPUTER ARCHITECTURE**
2	1	Objective, scope and outcome of the course.
3	**2**	**BASIC STRUCTURE OF COMPUTERS**
4	2	Functional units, software, performance issues software,
5	2	Machine instructions and programs
6	2	Types of instructions, Instruction sets: Instruction formats,
7	2	Assembly language, Stacks, Ques, Subroutines.
8	**3**	**PROCESSOR ORGANIZATION, INFORMATION REPRESENTATION**
9	3	Number formats. Multiplication & division, ALU design
10	3	Floating Point arithmetic, IEEE 754 floating point formats
11	3	Control Design
12	3	Instruction sequencing
13	3	Interpretation
14	**4**	**HARD WIRED CONTROL DESIGN METHODS AND CPU CONTROL UNIT.**
15	4	Microprogrammed Control - Basic concepts
16	4	Minimizing microinstruction size
17	4	Multiplier control unit
18	4	Microprogrammed computers - CPU control unit
19	**5**	**MEMORY ORGANIZATIONS**
20	5	Device characteristics, RAM, ROM, Memory management
21	5	Concept ofCache & associative memories,
22	5	Virtual memory.

23	**6**	**SYSTEM ORGANIZATION, INPUT - OUTPUT SYSTEMS**
24	6	Interrupt, DMA
25	6	Standard I/O interfacesConcept of parallel processing
26	6	Pipelining
27	6	Forms of parallel processing
28	6	Interconnect network

TEXT/REFERENCE BOOKS

1. Morris M. Mano, Computer Systems Architecture.3 ed, Prentice Hall India.
2. Carl Hamachar and Vranesic, Computer Organization, McGraw Hill.
3. John P. Hayes, Computer Architecture and Organization, TMH.
4. William stalling, Computer Organization and architecture, Pearson education.

NPTEL COUSES LINK

1. https://nptel.ac.in/courses/106/105/106105163/

QUIZ Link

1. https://www.sanfoundry.com/1000-computer-organization-architecture-questions-answers/

Assessment Methodology:

1. Two Midterm exams where student have to showcase subjective learning.
2. Final Exam (subjective paper) at the end of the semester.

5E1391

Roll No. _____ Total No of Pages: 2

5E1391

B. Tech. V - Sem. (Main / Back) Exam., Feb.-March - 2021
ESC Electronics & Communication Engineering
5EC 3–01 Computer Architecture

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 65

Min. Marks: 23

Instructions to Candidates:

Attempt all five questions from Part A, four questions out of six questions from Part B and one questions out of three from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[5×2=10]**

All questions are compulsory

Q.1 Distinguish pipelining from parallelism.

Q.2 How overflow occur in Subtraction?

Q.3 Define Computers Architecture.

Q.4 Differentiate DRAM and SRAM.

Q.5 What is meant by an interleaved memory?

PART – B

(Analytical/Problem solving questions) **[4×10=40]**

Attempt any four questions

Q.1 Is there any difference between RISC & CISC computers? Explain.

Q.2 What is the advantage of pipelining? Explain instruction pipeline in detail.

Q.3 Draw and explain the diagram of a DMA controller.

Q.4 What is need of Virtual Memory in the Computer System?

Q.5 Describe the procedure for addition and subtraction for fixed point number. Explain by use of flowchart.

Q.6 Explain various instruction formats.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[1×15=15]**

Attempt any one questions

Q.1 An address space is specified by 24 bits and the corresponding memory space by 16 bits –

(i) How many words are there in the address space?

(ii) How many words are there in the memory space?

(iii) If a page consists of 2K words, how many pages and block are there in the system?

Q.2 Explain the following terms with reference to Non – Von – Neumann machines.

(i) SISD

(ii) SIMD

(iii) MISD

(iv) MIMD

Q.3 What do you mean by parallel processing? Write the Flynn's classification of parallel processing.

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