**Techno India NJR Institute of Technology**



**Course File**

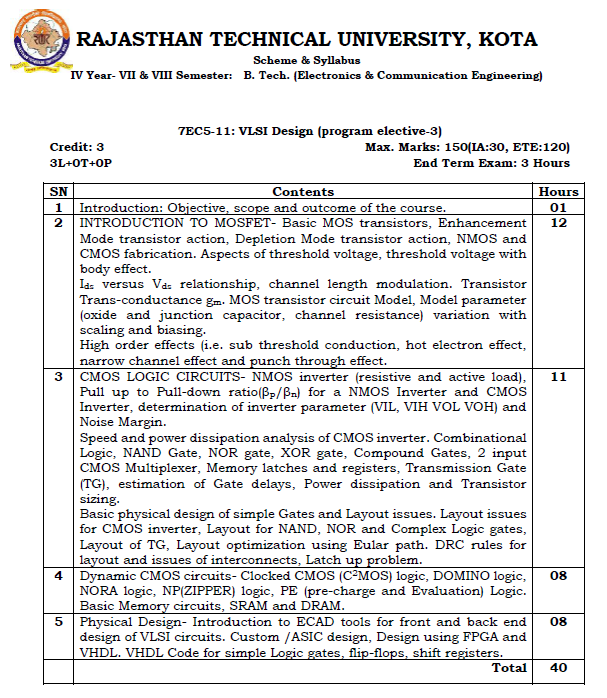
**Session 2020-21**

**VLSI Design (7EC5-11)**

Yogendra Singh Solanki

(Assistant Professor)

**Department of ECE**



**Course Overview:**

Student will learn fundamentals of VLSI design from this 40-hour course. In this course, student will study the fundamental concepts and structures of designing digital VLSI systems include CMOS devices and circuits, standard CMOS fabrication processes, CMOS design rules, static and dynamic logic structures, interconnect analysis, CMOS chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture.

**Course Outcomes:**

|  |  |  |
| --- | --- | --- |
| **CO.NO.** | **Cognitive Level** | **Course Outcome** |
| 1 | Analysis | Analyse and Simulate MOS Inverter characteristics. |
| 2 | Analysis | Analyse the various design parameters of CMOS circuits. |
| 3 | Synthesis | Design CMOS circuit & Layout. |
| 4 | Synthesis | Comprehend and design dynamic CMOS & Semiconductor Memories. |
| 5 | Synthesis | Design digital circuits using HDL |

**Prerequisites:**

1. Fundamentals of semiconductor devices.
2. Must have completed the course on Digital and Analog Electronics.
3. Student should be able to design any digital circuit for given requirements.

**Course Outcome Mapping with Program Outcome:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Outcome** | **Program Outcomes (PO’s)** | | | | | | | | | | | |
| **CO. NO.** | **Domain Specific** | | | | | **Domain Independent** | | | | | | |
|  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| CO1 | 2 | 1 | 1 | 0 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO2 | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO3 | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO4 | 2 | 1 | 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CO5 | 2 | 2 | 2 | 2 | 2 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High) | | | | | | | | | | | | |

**Course Coverage Module Wise:**

|  |  |  |
| --- | --- | --- |
| **Lecture No.** | **Unit** | **Topic** |
|  | **1** | **INTRODUCTION TO MOSFET** |
|  | 1 | Basic MOS transistors, Enhancement Mode transistor action, Depletion Mode transistor action. |
|  | 1 | NMOS and CMOS fabrication. |
|  | 1 | Aspects of threshold voltage, threshold voltage with body effect. |
|  | 1 | Ids versus Vds relationship, channel length modulation, Transistor Trans-conductance gm |
|  | 1 | MOS transistor circuit Model. |
|  | 1 | Model parameter (oxide and junction capacitor, channel resistance) variation with scaling and biasing. |
|  | 1 | High order effects |
|  | 1 | Sub-threshold conduction & hot electron effect, |
|  | 1 | Narrow channel effect and punch through effect. |
|  | **2** | **CMOS LOGIC CIRCUITS** |
|  | 2 | nMOS inverter (resistive and active load) |
|  | 2 | Pull up to Pull-down ratio for a NMOS Inverter |
|  | 2 | CMOS Inverter & Pull up to Pull-down ratio (Bn/Bp). |
|  | 2 | determination of inverter parameter (VIL, VIH VOL VOH) |
|  | 2 | Noise Margin. Speed and power dissipation analysis of CMOS inverter |
|  | 2 | Combinational Logic, NAND Gate, NOR gate, XOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers. |
|  | 2 | Transmission Gate, estimation of Gate delays, Power dissipation and Transistor sizing. |
|  | **3** | **BASIC PHYSICAL DESIGN OF SIMPLE GATES AND LAYOUT ISSUES** |
|  | 3 | Layout issues for CMOS inverter |
|  | 3 | Layout for NAND, NOR and Complex Logic gates |
|  | 3 | Layout of TG. |
|  | 3 | Layout optimization using Eular path. |
|  | 3 | DRC rules for layout |
|  | 3 | issues of interconnects |
|  | 3 | Latch up problem. |
|  | **4** | **DYNAMIC CMOS CIRCUITS** |
|  | 4 | Clocked CMOS (C2MOS) logic |
|  | 4 | DOMINO logic |
|  | 4 | NORA logic. |
|  | 4 | NP(ZIPPER) logic |
|  | 4 | PE(pre-charge and Evaluation) Logic |
|  | 4 | Basic Memory circuits |
|  | 4 | SRAM and DRAM |
|  | **5** | **PHYSICAL DESIGN** |
|  | 5 | Introduction to ECAD tools for front and back end design |
|  | 5 | Custom /ASIC design |
|  | 5 | Design using FPGA & VHDL |
|  | 5 | VHDL Code for simple Logic gates |
|  | 5 | VHDL Code for flip-flops, shift registers |

**TEXT/REFERENCE BOOKS**



**Teaching and Learning resources:**

* **MOOC (NPTEL): -** https://nptel.ac.in/courses/108/107/108107129/

**Assessment Methodology:**

1. Practical exam using Microwind VLSI design software.
2. Two Midterm exams where student have to showcase subjective learning.
3. Final Exam (subjective paper) at the end of the semester.

