Techno India NJR Institute of Technology

Course File

Signal & System (4EE4-08)

For Techno India NJR Institute of Technology
पंकज पोरवाल
Dr. Pankaj Kumar Porwal
(Principal)

Vivek Jain
(Associate Professor)
Department of ECE

RAJASTHAN TECHNICAL UNIVERSITY, KOTA

SYLLABUS

2nd Year - IV Semester: B.Tech. (Electrical Engineering)

4EE4-08: Digital Electronics

Credit: 2
2L+0T+0P

Max. Marks: 100(IA:20, ETE:80)
End Term Exam: 2 Hours

SN	CONTENTS	Hours
1	**Introduction:** Objective, scope and outcome of the course.	1
2	**Fundamentals of Digital Systems and logicfamilies:** Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital ICs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.	4
3	**Combinational DigitalCircuits:** Standard representation for logic functions, K-map representation, simplification of logic functions using K-map, minimization of logical functions. Don't care conditions, Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder, ALU, elementary ALU design, popular MSI chips, digital comparator, parity checker/generator, code converters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.	6
4	**Sequential circuits and systems:** A 1-bit memory, the circuit properties of Bistable latch, the clocked SR flip flop, J- K-T and D-types flip flops, applications of flip flops, shift registers, applications of shift registers, serial to parallel converter, parallel to serial converter, ring counter, sequence generator, ripple (Asynchronous) counters, synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.	6
5	**A/D and D/A Converters:** Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter, specifications for D/A converters, examples of D/A converter ICs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters, example of A/D converter ICs	4
6	**Semiconductor memories and Programmable logic devices** Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	7
	Total	28

Course Overview:

Digital electronics is a field of electronics involving the study of digital signals and the engineering of devices that use or produce them. Digital electronic circuits are usually made from large assemblies of logic gates, often packaged in integrated circuits.

Course Outcomes:

CO.NO.	Cognitive Level	Course Outcome
1	**Comprehension**	Verify the functionality of TTL ICs & understand the respective datasheet.
2	**Analysis**	Student able to analyze delay and power consumption of combinational logic circuits.
3	**Synthesis**	Design and develop sequential logic circuits such as counter, FSM.

Prerequisites:

1. Fundamentals knowledge of number system.
2. Fundamentals knowledge of diode and transistor.

Course Outcome Mapping with Program Outcome:

Course Outcome	Program Outcomes (PO's)											
CO. NO.	Domain Specific					Domain Independent						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	0	0	0	0	0	0	0	0
CO2	2	2	1	2	0	0	0	0	0	0	0	0
CO3	1	1	2	2	0	0	0	0	0	0	0	0
1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High)												

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Course Coverage Module Wise:

Lecture No.	Unit	Topic
1	**1**	**INTRODUCTION:** Objective, Scope And Outcome Of The Course.
2	**2**	**FUNDAMENTALS OF DIGITAL SYSTEMS AND LOGIC FAMILIES :** Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations.
3	2	Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number systems.
4	2	Binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes.
5	2	Characteristics of digital lCs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.
6	2	Practice Problems.
7	**3**	**COMBINATIONAL DIGITAL CIRCUITS:** Standard representation for logic functions, K-map representation.
8	3	Simplification of logic functions using K-map, minimization of logical functions. Don't care conditions.
9	3	Q-M method of function realization.
10	3	Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors.
11	3	BCD arithmetic, carry look ahead adder, serial adder, ALU, elementary ALU design.
12	3	Digital comparator, parity checker/generator, code converters.
13	3	Priority encoders, decoders/drivers for display devices.
14	**4**	**SEQUENTIAL CIRCUITS AND SYSTEMS :** A 1-bit memory, the circuit properties of Bi stable latch, the clocked SR flip flop.
15	4	J-K, T and D-types flip flops, Flip Flop Inter conversions
16	4	applications of flip flops, ripple (Asynchronous) counters
17	4	synchronous counters, counters design using flip flops,

18	4	Asynchronous sequential counters, applications of counters.
19	4	shift registers, applications of shift registers, serial to parallel converter, parallel to serial converter.
20	4	Ring counter, Twisted ring Counter, sequence generator
21	**5**	**A/D AND D/A CONVERTERS :** Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter.
22	5	Specifications for D/A converters, examples of D/A converter lCs, sample and hold circuit.
23	5	Analog to digital converters: quantization and encoding, parallel comparator A/D converter.
24	5	successive approximation A/D converter, counting A/D converter, dual slope A/D converter,
25	5	A/D converter using voltage to frequency and voltage to time conversion,
26	5	Specifications of A/D converters, example of A/D converter ICs.
27	**6**	**SEMICONDUCTOR MEMORIES AND PROGRAMMABLE LOGIC DEVICES** Memory organization and operation,
28	6	Expanding memory size, classification and characteristics of memories, sequential memory
29	6	Read only memory (ROM), read and write memory(RAM)
30	6	content addressable memory (CAM), charge de coupled device memory (CCD)
31	6	Commonly used memory chips, ROM as a PLD.
32	6	Programmable logic array, Programmable array logic
33	6	Complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).
34		Revision to course work.
35		Revision to course work.

TEXT/REFERENCE BOOKS

1. Digital Circuit & Logic Design, Morris Mano, Prentice Hall of India.

2.Digital Principles & Applications, A.P. Malvino& D.P. Leach, Tata Mc-graw Hill, Delhi.

NPTEL COUSES LINK

https://nptel.ac.in/courses/117/106/117106114/

QUIZ Link

https://rank.sanfoundry.com/digital-circuits-tests/

Faculty Notes Link

https://drive.google.com/drive/folders/1Yjw3QPnvqSjTQwUDME0emkdSLu7Tq3Jq?usp=sharing

Assessment Methodology:

1. Practical exam using MULTISIM software.
2. Two Midterm exams where student have to showcase subjective learning.
3. Final Exam (subjective paper) at the end of the semester.

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Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Find value of x for following equation:

$(135)_x + (531)_x = (666)_x$

Q.2 Convert $(1011)_{\text{gray code}}$ to excess-3 code.

Q.3 Find the sum of $(1.98)_{10} + (4.86)_{16}$.

Q.4 State the difference between flip flop and latch.

Q.5 Write the excitation table of RS flip flop.

Q.6 Define figure of merit for logic family.

Q.7 How many Boolean functions can be made from 3 variables?

Q.8 Write a VHDL code for $y=\overline{A}\overline{B}$ in structural style of modelling.

Q.9 How many flip flops are required to design modules 20 counter?

Q.10 If the present output of 4 – bit twisted ring counter is 1011, then find its output after 6 clock cycles.

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 How Ex-OR gate is used in parity bit generation and error detection at transmitter and receiver respectively? Explain using an example of 8-bit data.

Q.2 Convert following canonical form into standard form using tabulation method

$$Y=\sum m\,(4,5,6,11,13)+d\sum(0,2)$$

Q.3 Explain the procedure for conversion of RS flip flop into JK flip flop.

Q.4 Write the help of neat circuit diagram explain the interfacing of various logic families.

Q.5 Implement the following Boolean functions:

(i) $Y=\overline{AB+CD}$ using CMOS

(ii) $Y = AB+C$ using PMOS

Q.6 Write a VHDL code for full adder in structural style of modelling.

Q.7 What is FSM? State the difference between Mealy and Moore state machines.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 (a) What are prime, essential and redundant implicants? Explain with an example.

(b) Signals A, B, C, D and $\overline{A}$ are available. Using only 8:1 mux and no other gate, implement the expression F (A, B, C, D) = $B\overline{C} + AB\overline{D} + \overline{A}\,\overline{C}D$

Q.2 The state diagram of a FSM is given below (Fig 1).

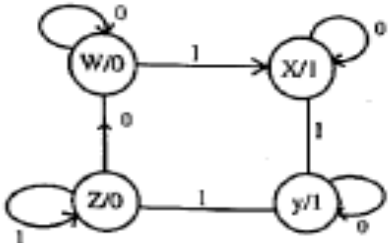

Fig 1

Show its state table, state assignment table and final implemented logic.

Q.3 Design a synchronous counter using JK flip flop to generate following sequence

0,7,5,3,2,1

Also write its state table, state assignment table and final implemented logic.

Q.4 (a) Design the 4-input priority encoder with truth table and draw its logic diagram.

(b) Draw and explain the logic diagram of BCD adder using two 4 bit adders and a correction detection circuit.

Q.5 Write a short note on following :

(i) FPGA

(ii) PLA

(iii) CPLD

(iv) PAL