Techno India NJR Institute of Technology

Department of Electronics & Communication Engineering

B.Tech. IV Semester

Lab: Analog Circuits Lab (4EC4-22)

4EC4-22: Analog Circuits Lab

Credit: 1.5 **Max. Marks: 75(IA:45, ETE:30)**

0L+0T+3P

List of Experiments	
Sr. No.	**Name of Experiment**
1.	Study and implementation of Voltage Series and Current Series Negative Feedback Amplifier.
2.	Study and implementation of Voltage Shunt and Current Shunt Negative Feedback Amplifier.
3.	Plot frequency response of BJT amplifier with and without feedback in the emitter circuit and calculate bandwidth, gain bandwidth product with and without negative feedback.
4.	Study and implementation of series and shunt voltage regulators and calculate line regulation and ripple factor.
5.	Plot and study the characteristics of small signal amplifier using FET.
6.	Study and implementation of push pull amplifier. Measure variation of output power & distortion with load and calculate the efficiency.
7.	Study and implementation of Wein bridge oscillator and observe the effect of variation in oscillator frequency.
8.	Study and implementation of transistor phase shift oscillator and observe the effect of variation in R & C on oscillator frequency and compare with theoretical value.
9.	Study and implementation of the following oscillators and observe the effect of variation of capacitance on oscillator frequency: (a) Hartley (b) Colpitts.
10.	Study and implementation of the Inverting And Non-Inverting Operational Amplifier.
11.	Study and implementation of Summing, Scaling And Averaging of Operational Amplifier
12.	Implementation of active filters using OPAMP.

Course Outcome:

Course Code	Course Name	Course Outcome	Details
4EC4-22	Analog Circuits Lab	CO 1	Discuss and observe the operation of a bipolar junction transistor and field-effect transistor in different region of operations.
		CO 2	Analyze and design of transistor Amplifier and Oscillators. Importance of negative feedback.
		CO 3	Analyze the frequency response of amplifiers and operational amplifier circuits. Develop an intuition for analog circuit behavior in both linear and nonlinear operation.
		CO 4	Design op-amps for specific gain, speed, or switching performance. Compensate operational amplifiers for stability.
		CO 5	Design and conduct experiments, interpret and analyze data, and report results.

CO-PO Mapping:

Subject	Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
4EC4-22 Analog Circuits Lab	CO 1	3	2	1	2	2							
	CO 2	2	3	1	2	3							
	CO 3	1	3	2	3	2							
	CO 4	1	2	3	2	3							
	CO 5	1	2	3	3	3							

3: Strongly **2: Moderate** **1: Weak**

Office of Dean Academic Affairs
Rajasthan Technical University, Kota

Course Outcomes:

CO1:	**Comprehension**	Classify and Descibe the operation of a bipolar junction transistor and field-effect transistor in different region of operations.
CO2:	**Application**	Illustrate the design of transistor Amplifier,Oscillators and Importance of negative feedback.
CO3:	**Analysis**	Analyze the frequency response of amplifiers and operational amplifier circuits. Develop an intuition for analog circuit behavior in both linear and nonlinear operation.
CO4:	**Synthesis**	Design op-amps for specific gain, speed, or switching performance. Compensate operational amplifiers for stability
CO5:	**Evaluation**	Design and conduct experiments, interpret and Evaluate data, and report results.

Course Outcome Mapping with Program Outcome:

CO1	2	1	2	1	1	1	0	0	0	0	1	2
CO2	2	0	2	0	1	1	0	0	0	0	2	1
CO3	2	0	1	0	2	1	0	0	1	0	2	2
CO4	1	0	1	0	1	2	1	0	1	0	1	2
CO5	0	0	2	2	2	2	1	0	0	0	2	2

Lab Ethics:

DO'S

1. Student should get the record of previous experiment checked before starting the new experiment.
2. Read the manual carefully before starting the experiment.
3. Before starting the experiment, get circuit diagram checked by the teacher.
4. Before switching on the power supply, get the circuit connections checked.
5. Get your readings checked by the teacher.
6. Apparatus must be handled carefully.
7. Maintain strict discipline.
8. Keep your mobile phone switched off or in vibration mode.
9. Students should get the experiment allotted for next turn, before leaving the lab.

DON'TS

1. Do not touch or attempt to touch the mains power supply wire with bare hands.
2. Do not overcrowd the tables.
3. Do not tamper with equipment's.
4. Do not leave the lab without permission from the teacher.

Safety Measures

1. Avoid direct contact with any voltage source and power line voltage. (Otherwise, and such contact may subject you to electrical shock).
2. Use insulating materials while working on electrical equipment.
3. Ensure that the power is OFF before you start connecting up the circuit. (Otherwise you will be touching the live parts in the circuit).
4. Check power chords for any sign of damage and be certain the chords use safety plugs and do not defeat the safety feature of these plugs by using ungrounded plugs.
5. When using connection leads, check for any insulation damage in the leads and avoid such defective leads.
6. Do not defeat any Safety devices such as fuse or circuit breaker by shorting across it. Switch on the power to your circuit and equipment only after getting them checked up and approved by the staff member.

Introduction about the Labs:

Analog circuits as the name suggests deals mainly with Analog signals. Analog electronic circuit design is one of the important and challenging fields in Electronics. The area of analog electronics is one of the vast and complex areas in VLSI circuit design. A signal which is having different values at different instants of time is referred to as an analog signal. Analog electronic circuits can be designed and tested for their performance using the tools like PSPICE, Cadence, etc.. Many analog circuits are available in the form of IC chips.

During this Lab course simple analog electronic circuits are designed using discrete components like Resistors, Capacitors, Inductors, PN junction diodes and Transistors (BJT's, FET's, etc.), etc.. These designed circuits are tested and verified for their performance under the laboratory conditions using power sources like DC Power supply, AC sources like function generators. Their input and output parameters like input waveforms, output waveforms, input and output current and voltage readings, the impedance or resistance offered by the circuit, etc. are analyzed by using measuring instruments like multimeter and CRO's. The captured values from the instruments are noted and used for further calculations.

The analog electronics laboratory course flows:

To start with, this laboratory session, initially all students is trained to use the measuring instruments like Multimeter and CRO. Thorough understanding of CRO is mandatory for proceeding with the courseware. The function or signal generators which generate the analog signals of desired frequency and amplitude (frequency and voltage levels) and usage of power supply etc. are made familiar to the students. Reading the values of the passive components like resistor, capacitor, etc. using color code is taught. After completing the above exercise, the design aspects of analog circuits are carried out. Thereafter the conduction of the experiments is starting to verify and test the performance of the designed analog circuits. The input and generated output waveforms are sketched and the results are noted for further calculations. Instructions to the students are given at the start of this document which they are advised to read before they start conducting experiments.

Instructions before Starting the Experiment

1. Students are expected to study the circuit, theory and procedures, expected output before doing the experiment.

2. Adjustment of signal generator: - Before connecting the signal generator to the circuit check the followings.

a. Set the shape of the waveform (sinusoidal),

b. Set the frequency using coarse and fine adjustments.

c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not , adjust it using the DC offsetting potentiometer

d. Set the voltage magnitude using V course settings and Vfine adjustments.

3. Adjustment of CRO:

a. Select the right voltage and time scale to get the proper waveform

b. For clipper and clamper circuits, observe the waveform in DC mode only

c. Set the input waveform mainly for offset setting in DC mode only.

d. Before measurement, ensure X & Y are in calibrated mode (if provided externally)

e. Ensure that Channel selection and trigger mode are properly set.

f. In case of two channels do not mix the signal and ground terminals.

4. Multi-meter adjustments:-

a. Set the right mode before taking the readings.

b. For current reading, connect the multimeter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for AC and DC modes as required.

c. For voltage reading ensures that proper AC or DC setting.

d. Use the proper leads for the measurement. Wrong cables damage the instrument.

5. After adjusting the input voltage, check the circuit connections before turning the power on.

6. Ensure that the circuit has one ground.

7. Don’t pull out the connections with the power supply on.

EXPERIMENT – 1

AIM: - (a) Design a Current series negative feedback amplifier of A_V=6 dB.

(b) Design a voltage series negative feedback amplifier of A_V=6 dB.

APPARATUS REQUIRED:

- Trainer kit of BJT Amplifier Model NO:-Aditron(4513)
- CRO (Dual Channel 20 MHz)
- Function Generator (1 MHz , 30Vpp)
- Power Supply 12V

COMPONENTS REQUIRED:-

Capacitor and resistors of desired values

THEORY:

The circuit topology in which part or all the output signal of an amplifier is re applied to the input terminal through a feedback network is referred as feedback.

If the phase of feed-back signal is same as that of input signals, this feedback is called positive feedback.If the phase of feed-back signal is inverse to that of input signals and this feedback signal will be subtracted from the input signal to reduce the gain, this feedback is called as negative feed back.

The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased.

In voltage series feedback amplifier, sampling is voltage and series mixing indicates voltage mixing. As both input and output are voltage signals and is said to be voltage amplifier with gain A_{vf}.

In voltage series Feedback amplifier, the input impedance and the output impedance are increased. Noise and distortions are reduced considerably.

The current series feedback amplifier is also called as series fed amplifier or transconductance amplifier. When the part of the output current is sampled and given to the feedback circuit, where the fraction of the current is converted into a proportional voltage and then given as input signal.

Bandwidth is defined as the range frequencies over which gain is greater than or equal to 0.707 times the maximum gain or up to 3 dB down from the maximum gain.

$$\text{Bandwidth (BW)} = f_h - f_l$$

Where:

f_h= Upper cutoff frequency

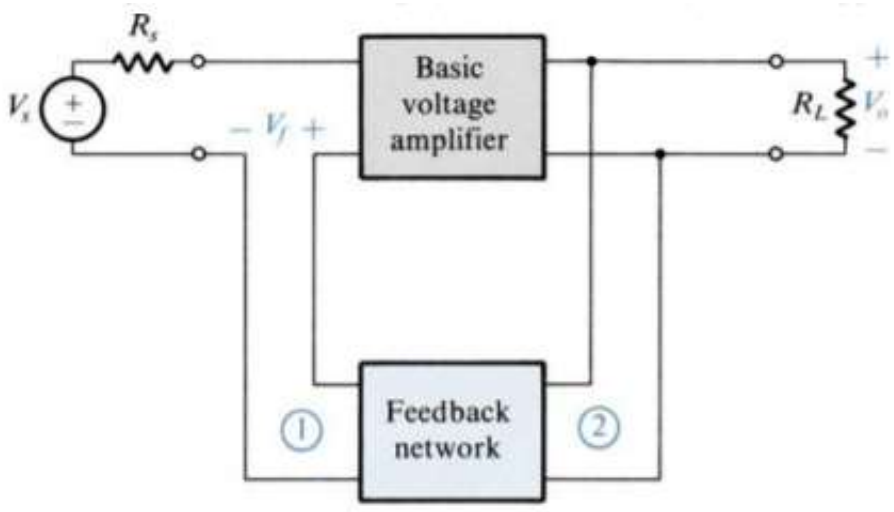
f_l = Lower cutoff frequency.

The cutoff frequency is the frequency at which the gain is 0.707 times the maximum gain or 3dB down from the maximum gain.In all feedback amplifiers we use negative feedback, so the gain is reduced and bandwidth is increased

$$A_f = A/(1+BA)$$

For negative feedback BA<1 (BA>-1)

For positive feedback BA<1 (BA<-1)



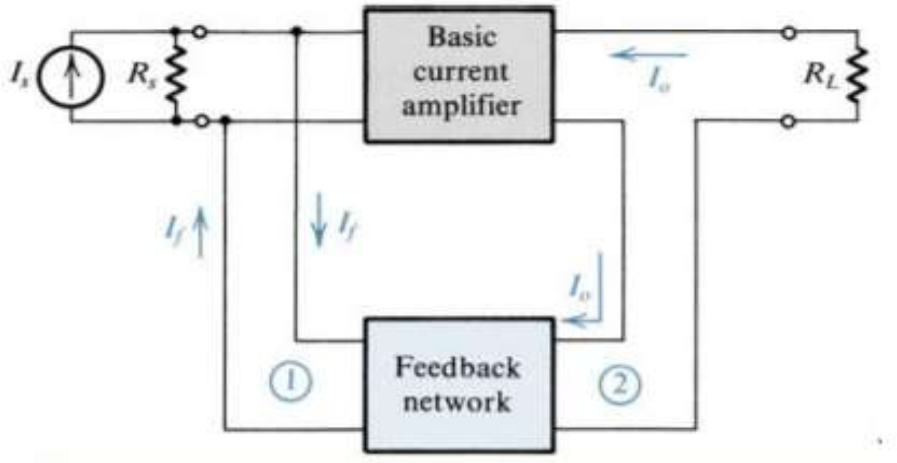


Fig 1.1 Block Diagram of Voltage Series feedback amplifier and current series feedback amplifier

Current Series feedback amplifier:

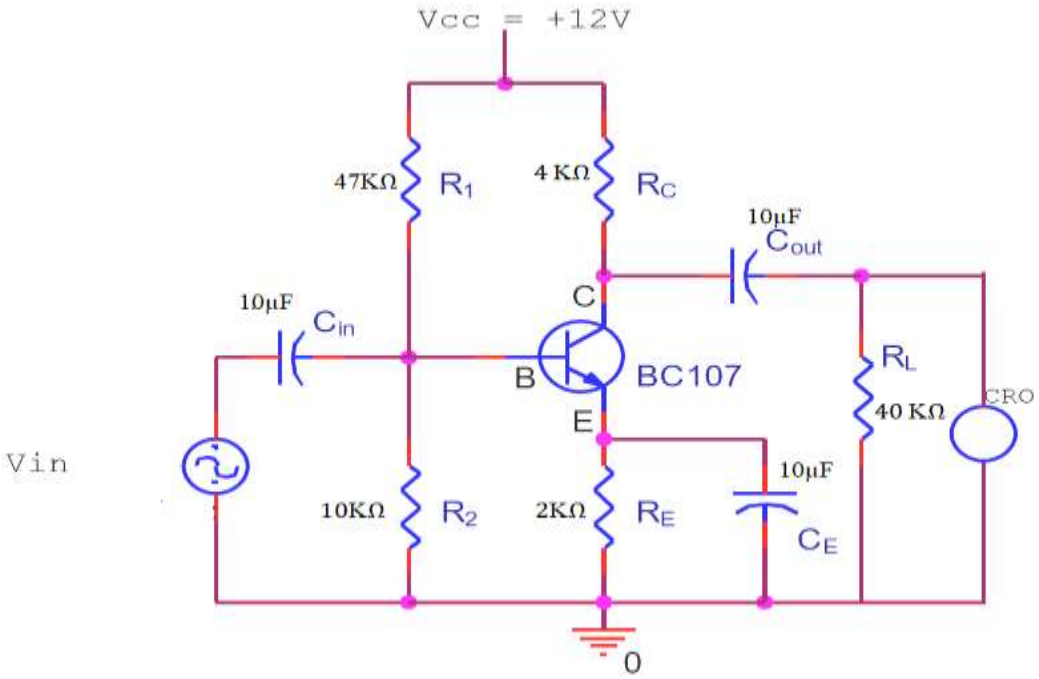


Fig. 1.2 Current series amplifier without feedback

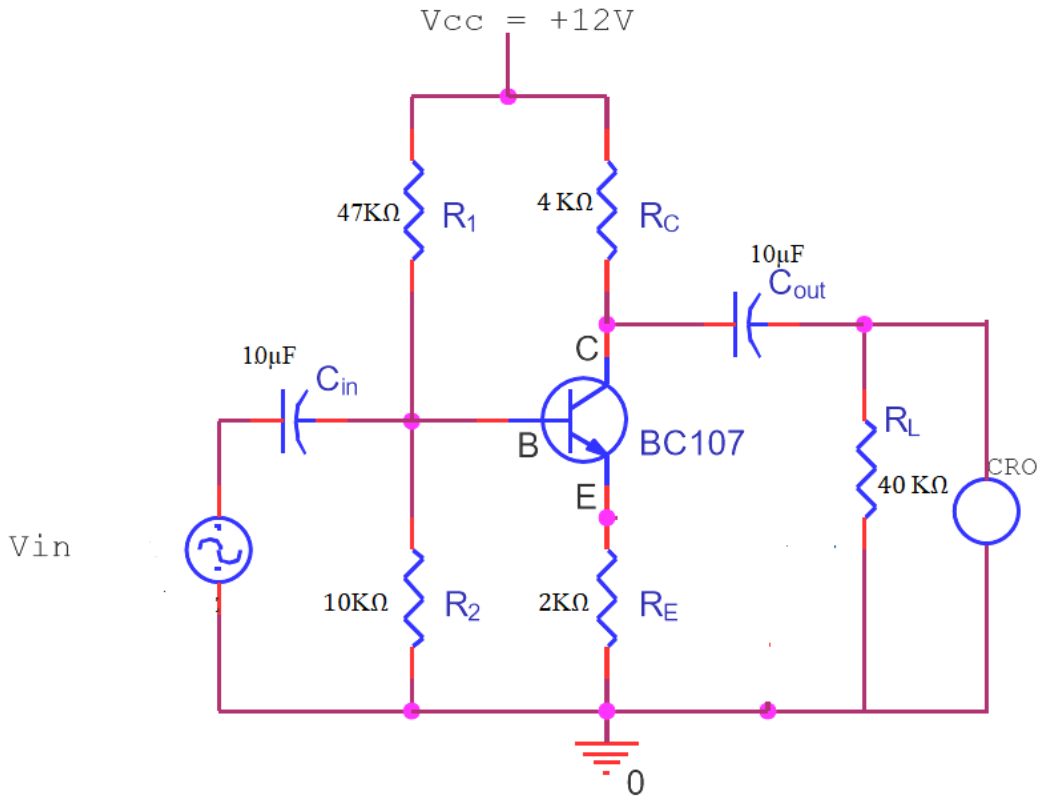


Fig. 1.3 Current series amplifier without feedback

DESIGN PROCEDURE:

Current Series feedback amplifier

Let V_{CC}=12V, I_C=1mA, Av=6dB, R_f=2.5KΩ,S=5,R_L=40KΩ

Find R_C,R_E and R_1,R_2

We know that $V_{CE} = \frac{V_{CC}}{2} = \frac{12}{2} = 6V$

$$A_V \cong -\frac{R_C}{R_E}$$

A_V=6dB or Av=2

R_C=2R_E……..(1)

V_{CC}=$I_C R_C$+V_{CE}+$I_E R_E$

12=1xR_C+6+1xR_E

R_C+R_E=6……..(2)

R_E=2KΩ and R_C= 4KΩ

$S \cong 1+\frac{R_B}{R_E} = 5 = 1+\frac{R_B}{2}$

R_B=8 KΩ

$R_B=\frac{R_1R_2}{R_1+R_2}$ =8 KΩ……(3)

So R_1=47KΩ & R_2=10KΩ

Consider: $C_f=C_{in}$=10µF, C_E=10 µF, C_{out}= 10 µF

$\beta=\frac{R_E}{R_C}$ =2

$A_f=\frac{A}{1+A\beta}=\frac{2}{1+2X2}$ = 0.4

Volatge Series Feedback amplifier:

Without feedback:

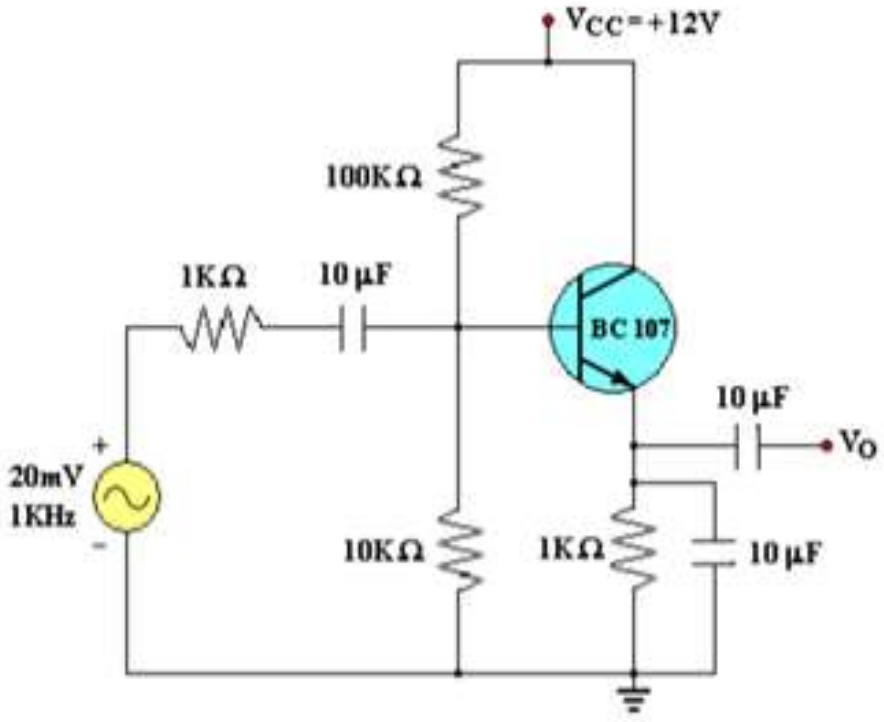


Fig. 1.4 Voltage series feedback amplifier (without feedback)

With feedback:

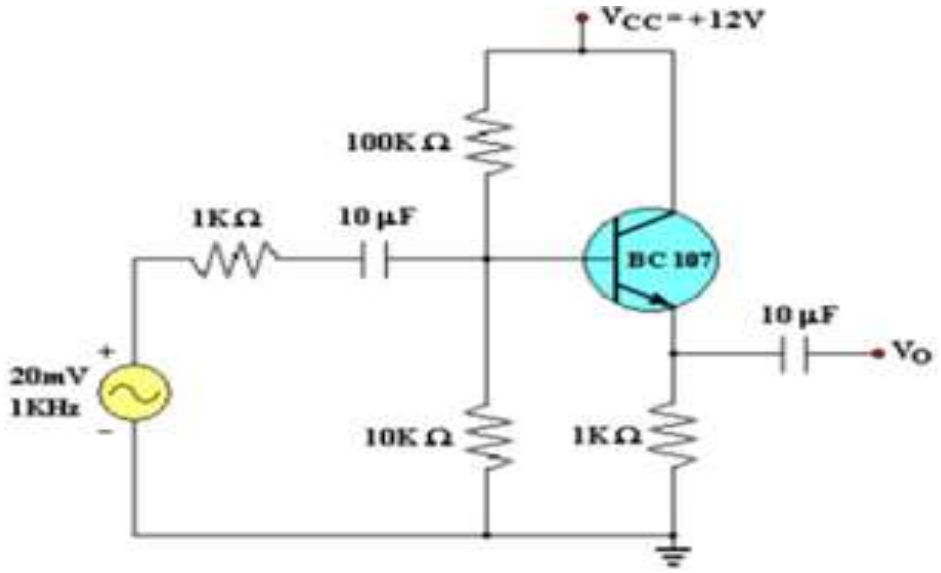


Fig. 1.5 Voltage series feedback amplifier (with feedback)

Voltage series feedback amplifier

Open loop gain or gain without feedback A=2

$\beta=\frac{V_f}{V_o}=1$

So Gin with feedback$A_f = \frac{A}{1+A\beta}=\frac{2}{1+2} = 0.67$

PROCEDURE:

I. Calculate the desired value of component as per given calculation.

II. Connections are made as per circuit diagram Fig. 2.2

III. Keep the input voltage constant at 50mV peak-peak and 1 KHz frequency. Note down the output voltage and calculate the gain by using the expression
Av=20 log(Vo/Vi) db

IV. See the waveform at CRO with feedback and without feedback.

OBSERVATION:

Current Series feedback amplifier

Table 1.1: Gains at 1 KHz

V_{in}	Frequency	V_{out}(With f/b)	V_{out} (Without f/b)	Gain(With f/b)	Gain(Without f/b)
50mV	1×10^3				

Voltage series feedback amplifier

Table 1.1: Gains at 1KHz

V_{in}	Frequency	V_{out}(With f/b)	V_{out} (Without f/b)	Gain(With f/b)	Gain(Without f/b)
50mV	1×10^3				

RESULT:- We have successfully designed of a current series and voltage series feedback amplifier of A_V=6 dB.

We have calculated the value of the required component:

R_E=2KΩ and R_C= 4KΩ, R_1=47KΩ & R_2=10KΩ

So the current series and voltage series feedback amplifier is implemented and gain at 1KHz are compared with & without feedback.

DISCUSSION:

1. What is positive and negative feedback?
2. What is the application of feedback amplifier?
3. What are the demerits of negative feedback?
4. Define current gain and voltage gain
5. Why the bandwidth of a circuit increases with feedback

EXPERIMENT – 2

AIM: - (a) Design a voltage shunt feedback amplifier of A_V=6 dB and a feedback resistance 2Ω.

(b) Design a current shunt feedback amplifier of A_V=6 dB and a feedback resistance 2Ω.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Bread board with power supply (±12V).

COMPONENTS REQUIRED:-

Capacitor and resistors of desired values

THEORY:

Feedback plays a very important role in electronic circuits and the basic parameters, such as input impedance, output impedance, current and voltage gain and bandwidth, may be altered considerably by the use of feedback for a given amplifier. A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal and thereby the feedback is accomplished.

There are two types of feedback. They are i) Positive feedback and ii) Negative feedback. Negative feedback helps to increase the bandwidth, decrease gain, distortion, and noise, modify input and output resistances as desired. An amplifier circuit equipped with some amount of negative feedback is not only more stable, but it distorts the input waveform less and is generally capable of amplifying a wider range of frequencies. The tradeoff for these advantages (there just has to be a disadvantage to negative feedback, right?) is decreased gain. If a portion of an amplifier's output signal is “fed back” to the input to oppose any changes in the output, it will require a greater input signal amplitude to drive the amplifier's output to the same amplitude as before. This constitutes a decreased gain. However, the advantages of stability, lower distortion, and greater bandwidth are worth the tradeoff in reduced gain for many applications.

Voltage shunt feedback is also called a shunt derived shunt feedback connection. Here a fraction of the output is supplied in parallel with input voltage through the feedback network. This type of amplifier is also called as transresistance amplifier.

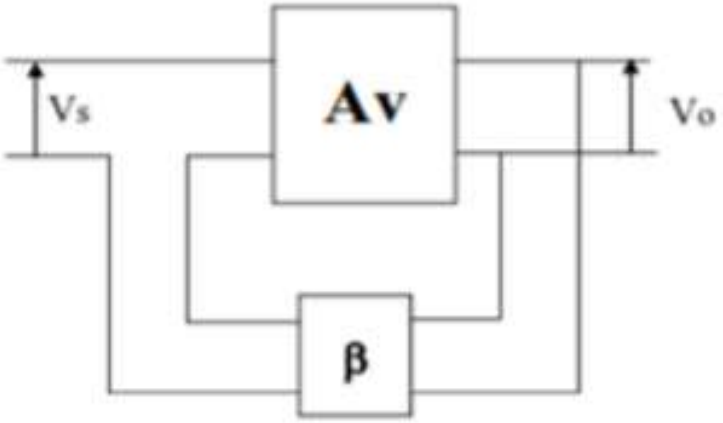


Fig. 2.1 Block diagram of Voltage shunt feedback amplifier

A current shunt feedback amplifier circuit is illustrated in the figure 1. It is called a series-derived, shunt-fed feedback. The shunt connection at the input reduces the input resistance and the series connection at the output increases the output resistance. This is a true current amplifier.

Current shunt feedback amplifier:

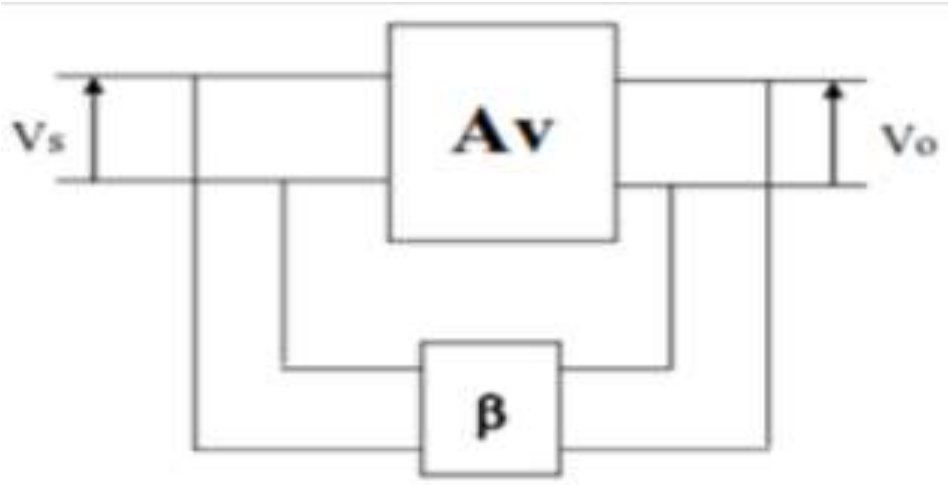


Fig. 2.2 Block diagram of Current shunt feedback amplifier

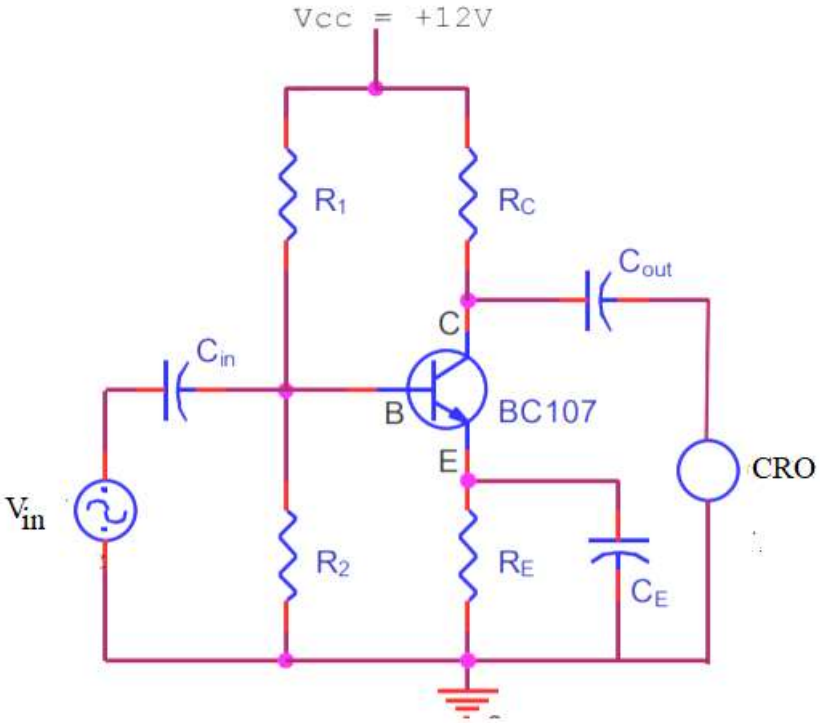


Fig. 2.3 Voltage Shunt feedback amplifier (without feedback)

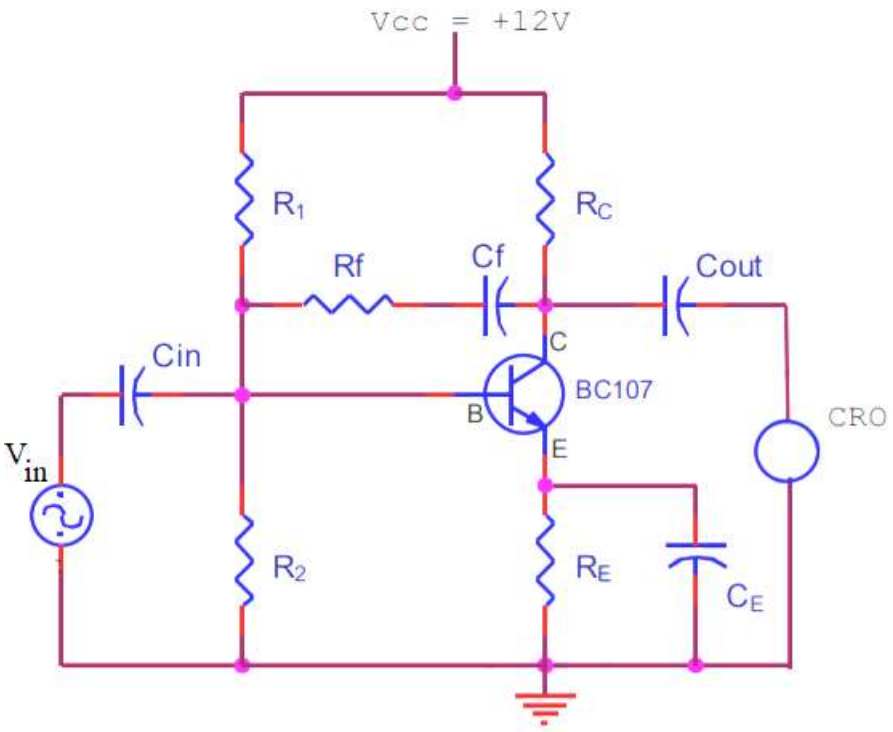


Fig. 2.4 Voltage Shunt feedback amplifier (with feedback)

DESIGN PROCEDURE:

Voltage shunt feedback amplifier

Let V_{CC}=12V, I_C=1mA, Av=6dB, R_f=2.5KΩ,S=2,R_F=2 Ω

Find R_C,R_E and R_1,R_2

We know that $\frac{V_{CC}}{2} = \frac{12}{2} = 6V$

$$A_V = -\frac{R_C}{R_E}$$

A_V=6dB or Av=2

R_C=2R_E……..(1)

V_{CC}=$I_C R_C$+V_{CE}+$I_E R_E$

12=1xR_C+6+1xR_E

R_C+R_E=6……..(2)

R_E=2KΩ and R_C= 4KΩ

S=1+$\frac{R_B}{R_E} = 5$ =1+$\frac{R_B}{2}$

R_B=8 KΩ

R_B=$\frac{R_1 R_2}{R_1+R_2}$ =8KΩ ……(3)

So R_1=47KΩ & R_2=10KΩ

Consider : C_f=C_{in}=10µF, C_E=10 µF, C_{out}= 10 µF

If R_F=2 Ω then β = $\frac{1}{R_F}$ =0.5

A_f = $\frac{A}{1+A\beta}$ =$\frac{2}{1+2X0.5}$ = 1

Circuit diagram of current shunt feedback amplifier:

Without feedback amplifier:

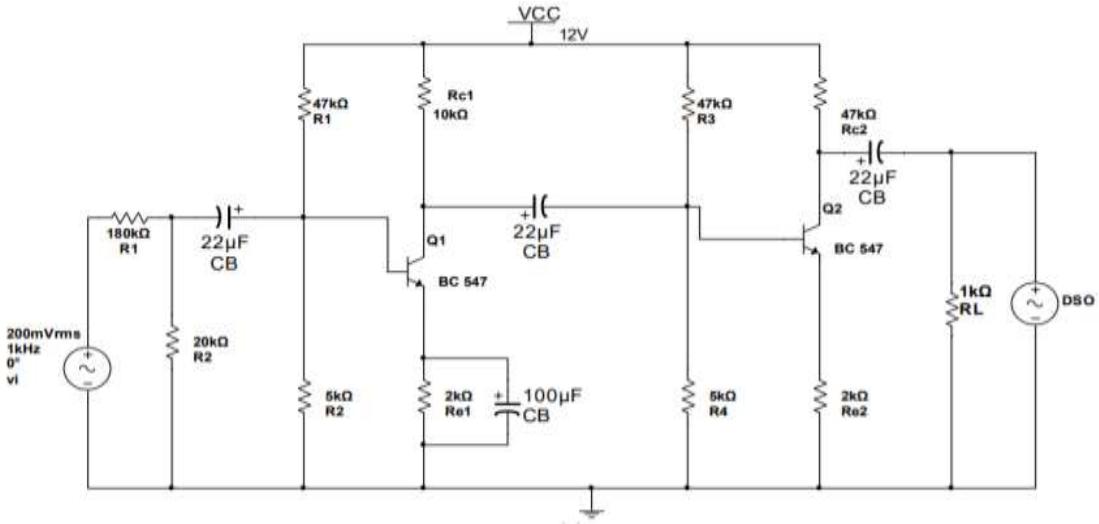


Fig. 2.5 Current Shunt feedback amplifier (without feedback)

With feedback:

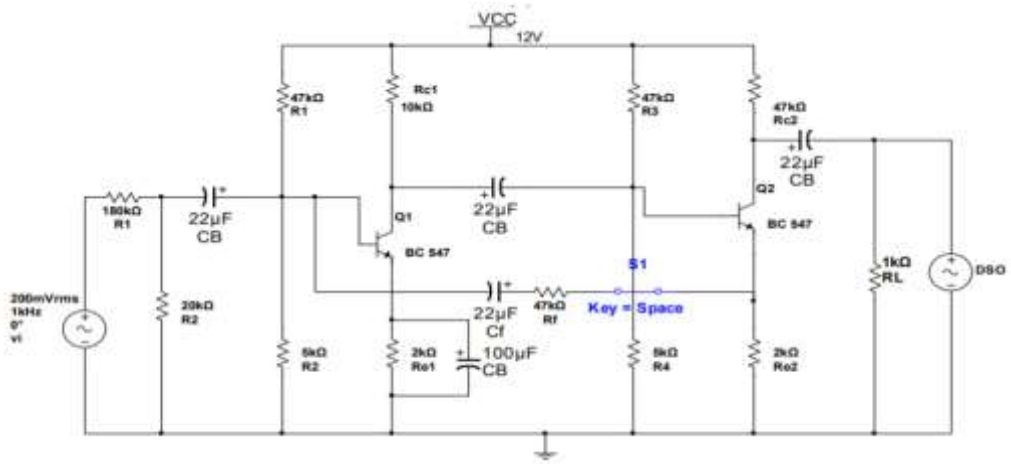


Fig. 2.6 Current Shunt feedback amplifier (with feedback)

Current shunt feedback amplifier:

Open loop gain or gain without feedback A=2

$$B = \frac{I_f}{I_o} = \frac{R_e}{R_e+R_f} = \frac{2}{2+47} = 0.041$$

So Gin with feedback $A_f = \frac{A}{1+A\beta} = \frac{2}{1+2\times0.041} = 1.84$

PROCEDURE:

I. Calculate the desired value of component as per given calculation.

II. Connections are made as per circuit diagram Fig. 2.2

III. Keep the input voltage constant at 50mV peak-peak and 1 KHz frequency. Note down the output voltage and calculate the gain by using the expression
Av=20 log(Vo/Vi) db

IV. See the waveform at CRO with feedback and without feedback.

OBSERVATION:

Voltage Shunt feedback amplifier

Table 2.1: Gains at 1KHz

V_{in}	Frequency	V_{out}(With f/b)	V_{out} (Without f/b)	Gain(With f/b)	Gain(Without f/b)
50mV	1×10^3				

Current Shunt feedback amplifier

Table 2.2: Gains at 1KHz

V_{in}	Frequency	V_{out}(With f/b)	V_{out} (Without f/b)	Gain(With f/b)	Gain(Without f/b)
50mV	1×10^3				

RESULT:- We have successfully designed of a voltage shunt and Current Shunt feedback amplifier of A_V=6 dB.

We have calculated the value of the required component:

R_E=2KΩ and R_C= 4KΩ, R_1=7KΩ & R_2=3KΩ

So the Voltage shunt Current Shunt feedback amplifier is implemented and gain at 1KHz are compared with & without feedback.

DISCUSSION:

1. What are the feedback and sampled signal in voltage shunt feedback amplifier.
2. What are the feedback and sampled signal in current shunt feedback amplifier.
3. What are the merits of negative feedback?
4. What are the effect of negative feedback amplifier in bandwidth.?
5. What are the application of voltage shunt and current shunt feedback amplifier.

EXPERIMENT-3

AIM:-Design a two stage RC coupled BJT amplifier with and without feedback in the emitter circuit at lower cut off frequency of 27 Hz and upper cut off frequency of 20 kHz with mid band gain (A_{vm}) of 32.15dB. Plot the frequency response of the amplifier and calculate the gain bandwidth product.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board (+12V & -12V)

COMPONENT REQUIRED:-

Capacitors and resistors of desired values, BJT (BC 107).

THEORY:

When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor R_C. It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in db. The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor Cc and at high frequencies due to junction capacitance C_{BE}.

This is most popular type of coupling as it provides excellent audio fidelity. A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R_1, R_2, R_E form biasing and stabilization network, Emitter bypass capacitor offers low reactance paths to signal, Coupling Capacitor transmits ac signal & blocks DC. Cascade stages amplify signal and overall gain is increased. Total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to $A=A1\times A2$

A_1=voltage gain of first stage, A_2=voltage gain of second stage.

Voltage Gain in (dB)

$$A(dB) = 20 \log_{10} \left(\frac{\mathbf{Vout}}{\mathbf{Vin}}\right)$$

CIRCUIT DIAGRAM:-

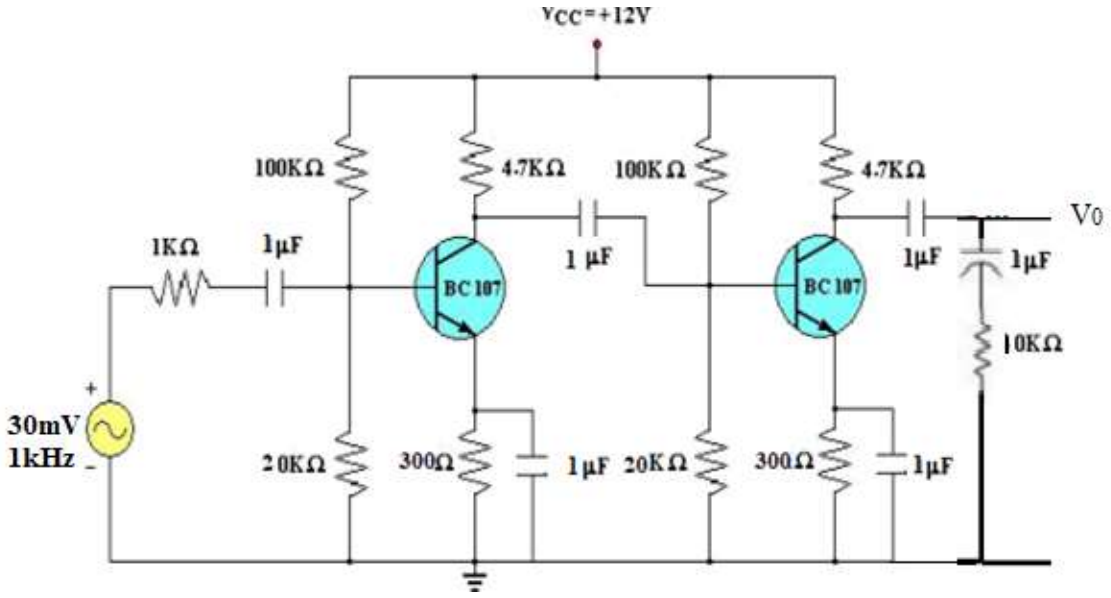


Fig.:3.1 BJT amplifier with feedback

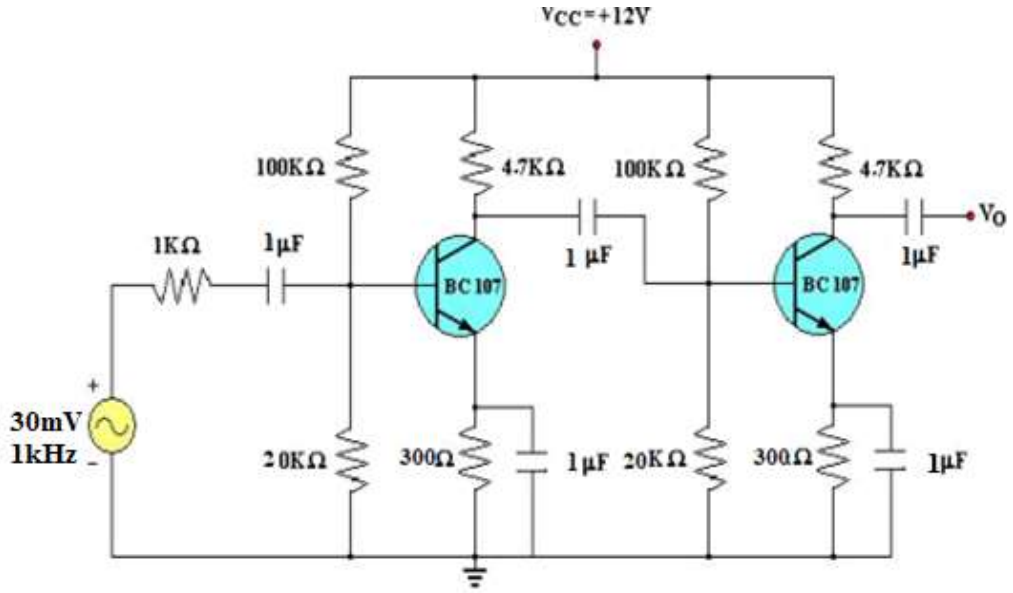


Fig.:3.2 BJT amplifier without feedback

DESIGN PROCEDURE:

Given mid band gain (A_{vm})= 32.15dB

Let h_{ie}=1.1kΩ, h_{fe}= 50 Ω

$20\log_{10}(x) = 32.15$ dB

X= 40.15

$$A_{vm} = \frac{h_{fe}R_C}{h_{ie} + R_C}$$

$$40.51 = \frac{50 \times R_C}{1.1 \times 10^3 + R_C}$$

R_C= 4.7kΩ

Since we need to design a filter with lower cut off frequency(f_L) of 27 Hz and upper cut off frequency(f_H) of 20kHz

$$f_L = \frac{1}{2\pi C_C(h_{ie} + R_C)}$$

$$27 = \frac{1}{2\pi C_C(1.1 \times 10^3 + 4.7 \times 10^3)}$$

$C_C = 1 \times 10^{-6}$

Let operating point Q :(I_C = 2mA, V_{CE} = 2V), V_{CC} = 12V, β=200, C_E=1μF

Determine the values of R_1, R_2 and R_E.

$$I_C = \beta I_B \Rightarrow I_B = \frac{2 \times 10^{-3}}{200} \Rightarrow I_B = 10 \times 10^{-6}$$

$I_1 = 10 \times I_B$

$I_1 = 100 \times 10^{-6}$

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$100 \times 10^{-6} = \frac{12}{R_1 + R_2}$$

$R_1 + R_2 = 120 \times 10^3$

Let R_F = 10kΩ

$V_{CE} = V_C - V_E$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$ ……(I_C=I_E)

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

$2 = 12 - 2\times10^{-3}(4.7\times10^{3} + R_E)$

$R_E = 300\Omega$

C_F will be same as C_C.

$C_F = 1\times10^{-6}$

PROCEDURE:

1. To design an amplifier, find the value R_C & C_C from the given values of mid band gain (A_{vm}) & lower cut off frequency(f_L)
2. Next we have to calculate the values of R_1, R_2 and R_E from V_{CE} & I_C.
3. Apply input to the circuit by using function generator.
4. Observe the output on CRO by varying the frequency of input signal from function generator.
5. Calculate gain in dB using given equation.
6. Plot the frequency response curve between gain and frequency.

OBSERVATION:

Vin: 30 mV

Table 3.1 Voltage gain change with frequency

S.No.	Frequency (Hz)	V_{out}(V)	Voltage Gain(V_o/V_i)	Voltage Gain in dB ($20 \log_{10} V_o/V_i$)
1	27			
2	50			
3	70			
4	100			
5	500			

6	1×10^3			
7	10×10^3			
8	100×10^3			
9	300×10^3			
10	500×10^3			
11	700×10^3			
12	1×10^6			

Bandwidth=Upper cut of frequency(f_L)-Lower cut off frequency (f_H)

FREQUENCY RESPONSE:

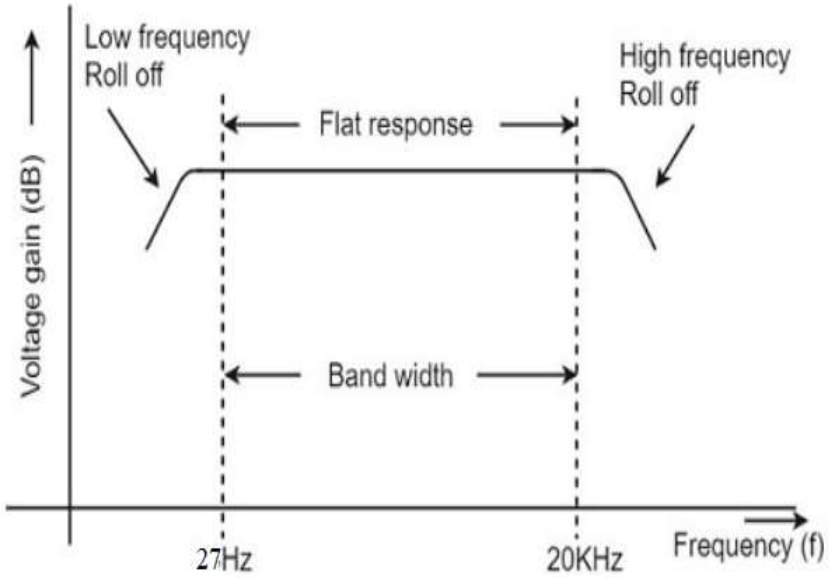


Figure 3.3: Frequency response

RESULT:-

We have successfully designed a two stage RC coupled amplifier using BJT (BC 107) at a lower cut off frequency 27 Hz and upper cut off frequency of 20 kHz with mid band gain of 32.15dB.

Designed parameters are as follows:

R_E= 300Ω, C_C= 1×10^{-6}, C_F = 1×10^{-6}, R_F = 10kΩ, R_C= 4.7kΩ, $R_1+R_2=120\times10^3$

We have plotted the frequency response curve for the designed amplifier. As per the frequency response curve, the gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. Thus Bandwidth is calculated with the help of upper and lower cut off frequency.

	Lower cut off frequency	Upper cut off frequency
Theoretical value		
Practical value		
Error		

DISCUSSION:

1. What is the necessity of cascading?
2. Why RC coupling is preferred in audio range?
3. In RC coupled amplifier why gain is decreased at high and low frequency ranges?
4. What do you mean by operating point?
5. Define what is the effect of removal of bypass capacitor in a CE amplifier circuit?
6. Why common collector circuit is known as an emitter follower?

EXPERIMENT– 4

AIM: (a) Design a series voltage regulator circuit a to provide output of 9V for a maximum of load current of 1 A, when the input variation is 15 V to 18 V and transistor gain is 50.

(b)Design a shunt regulator using a transistor and a Zener diodes required to maintain output voltage constant at 10V.The emitter current is limited to 100mA, input voltage is 12.5±10% and V_{BE}=0.4 V.

APPARATUS REQUIRED:

- DC Voltmeter Moving coil (0-20V)
- Power Supply (0-30V)
- Bread Board

COMPONENTS REQUIRED:

Zener diode, Transistor(BC546), desired value of Resistors

THEORY:

The Voltage regulator is a device designed to maintain the output voltage as nearly constant as possible. It monitors the output voltage and generates feedback that automatically increases and decreases the supply voltage to compensate for any changes in output voltage that might occur because of change in load are changes in load voltages.

Series voltage regulator:

In series voltage regulator the control element is a transistor which is in series with load. Must be operated in reverse break down region, where it provides constant voltage irrespective of changes in applied voltages. The output voltage of the series voltage regulator is $V_o = V_z - V_{BE}$.

Since, V_z is constant; any change in V_o must cause a change in V_{BE} in order to maintain the above equation. So, when V_o decreases V_{BE} increases, which causes the transistor to conduct more and to produce more load current, this increase in load causes an increase in V_o and makes V_o as constant. Similarly, the regulation action happens when V_o increases also.

Shunt voltage regulator:

A voltage regulator is a device or a combination of devices, design to maintain the output voltage of a power supply as nearly constant as possible even if there are changes in load or in input voltage. In shunt voltage regulator transistor Q acts as control element, which is in shunt with load voltage.

The output voltage is given as

$$V_o = V_z + V_R = V_z + V_{be}$$

Load regulation:

Load regulation refers to the amount the output voltage changes between the no-load and full-load conditions. Load regulation is one method used to determine the relative quality or effectiveness of a voltage regulator to maintain nominal (or no-load) regulation. The lower the load regulation, the better the regulator is in keeping the output voltage at its nominal value (the no-load voltage) for a particular load.

Percentage load Regulation = $\frac{V_{NL}-V_{FL}}{VFL}$ $\boldsymbol{X100}$

V_{NL}=Load voltage at no load

V_{FL}=load voltage at full load

Line regulation:

Line regulation is the variation in output voltage (ΔVo) that occurs when the line voltage (the unregulated input voltage V_{LN}) increases or decreases by a specified amount.The lower the line regulation, the better the regulator is in keeping the output voltage constant when changes in line voltage occur.

Percentage Line Regulation = $\frac{\Delta V_0}{\Delta V_i}$x 100

ΔV_0=change in output voltage

ΔV_I=change in input voltage

PROCEDURE:-

I. Calculate the component value and specification of transistor and diode for the required output.
II. Connections are made as per the circuit diagram.
III. Measure the output voltage with the load resistance.

IV. Measure the output voltage to the input voltage.

V. Calculate the load regulation and line regulation factor.

CIRCUIT DIAGRAM:-

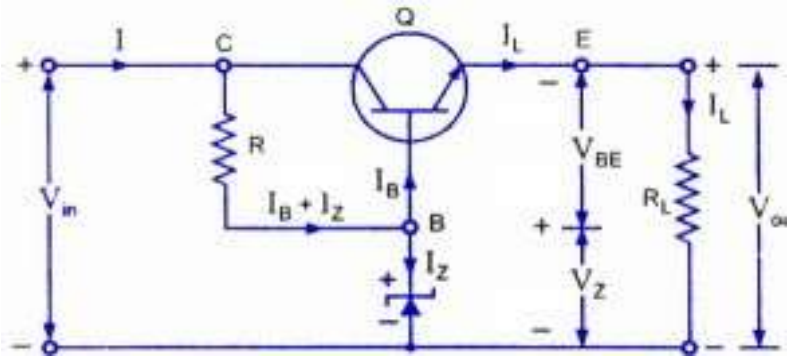


Fig 4.1: Series Voltage Regulator

DESIGN PROCEDURE:

Given: Load current I_L:1A, Vo=9V, V_i=15 V-18V, β=50

In series regulator:$I_E=I_L$=1A ,β=50

$$I_B=\frac{I_E}{\beta+1}=\frac{1}{50+1}=20\ mA$$

Let I_Z (min) =5mA

$V_{out}=V_Z-V_{BE}$

Zener diode breakdown voltage $V_Z=V_{out}+V_{BE}$=9+0.7=9.7V

Minimum current through resistor R:

$I_{R(min)}=I_{Z(min)}+I_B$=5+20=25 mA

$$R=\frac{V_{in(min)}-V_Z}{I_{R(min)}}=\frac{15-9.7}{25\ X\ 10^{-3}}=210\ \Omega$$

Maximum current through resistor R

$$I_R(max)=\frac{V_{in(max)}-V_Z}{R}=\frac{18-9.7}{210}=39.52\ mA$$

So maximum current through Zener diode

$I_Z(max)=I_R(max)-I_B$=39.52-20=19.52 mA

Power rating of Zener diode

$P_Z=V_ZI_Z(max)$=9.7 ***X*** 19.52=189.34 mW

Select Zener diode with the specification

Vz=10V and Pz=0.2 W

And transistor with specification of

V_{CEO}=20 V, I_C (max) =1 A and β=50

OBSERVATION:-

Table 4. 1: Observation table of Load Regulation

V_{in}=15V

S. No.	R_L	Output Voltage V_o
1	0	
2	1 KΩ	
3	2 KΩ	
4	3 KΩ	
5	4 KΩ	
6	5 KΩ	
7	6 KΩ	
8	7 KΩ	
9	8 KΩ	
10	9 KΩ	

Table 4.2: Observation Table for Line Regulation

S.No.	V_{in}	V_{out}
1.	0	
2.	2	
3.	4	
4.	6	
5.	8	
6.	10	
7.	12	
8.	14	
9	16	
10	18	

Percentage load Regulation = $\frac{V_{NL}-V_{FL}}{VFL}$ $\boldsymbol{X100}$

V_{NL}=Load voltage at no load

V_{FL}=load voltage at full load

Percentage Line Regulation = $\frac{\Delta V_0}{\Delta V_i}$x 100

ΔV_0=change in output voltage

ΔV_I=change in input voltage

SHUNT REGULATOR:

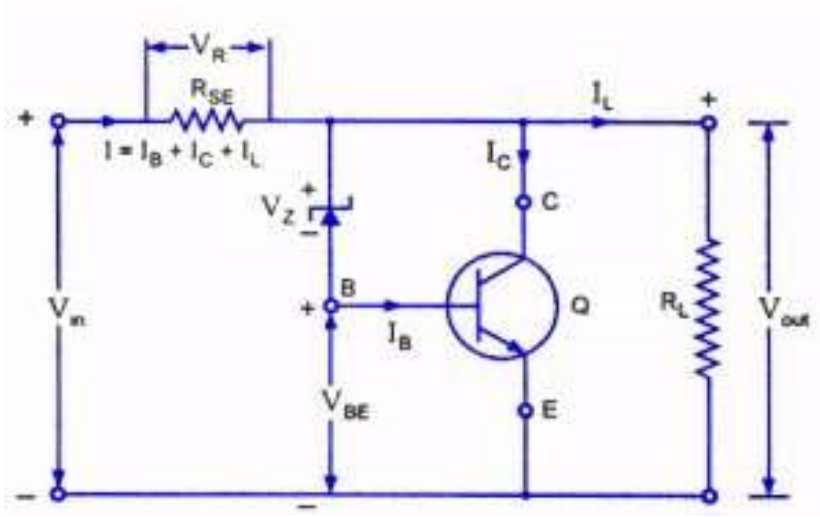


Fig 4.2: Shunt Voltage Regulator

Design calculation for shunt regulator:

Output voltage: V_{out}=10V,V_{BE}=0.7V,V_{in}=12.5±10%, I_E=100mA

$V_Z=V_{out}-V_{BE}$=10-0.7=9.3V

Input Voltage V_i= 12.5±10%=11.25V-13.75V

Minimum voltage to be dropped in series resistor R_{se}=11.25-10=1.25V

Maximum load current I_L=200mA

Required series resistance $R_{se}=\frac{1.25}{0.2}$ =6.25 **Ω**

Select Zener diode with the specification

V_z=9.3V, R_{se}=12.5 Ω

And transistor with specification of

I_C=100mA,β=100

V_{in}=12V

Table 4.3: Observation table of Load Regulation

S. No.	R_L	Output Voltage V_o
1	0	
2	1 KΩ	

3	2 KΩ	
4	3 KΩ	
5	4 KΩ	
6	5 KΩ	
7	6 KΩ	
8	7 KΩ	
9	8 KΩ	
10	9 KΩ	

Table 4.4: Observation Table for Line Regulation

S.No.	**V_{in}**	**V_{out}**
1.	0	
2.	2	
3.	4	
4.	6	
5.	8	
6.	10	
7.	12	
8.	14	
9	16	
10	18	

RESULT:- We have successfully designed a series voltage regulator using a transistor to provide output of 9V for a maximum of load current of 1 A, when the input variation is 15 V to 18 and Load variation.

We have found the specification of the component:

Zener diode with the specification: Vz=10V and Pz=0.2 W

Transistor with specification: VCEO= 20 V, I_C (max) =1 A and β=50

We have successfully designed a shunt regulator using a transistor and a Zener diode required to maintain output voltage constant at 10V, 100 mA and when the input variation is 12.5±10% and Load variation.

We have found the specification of the component:

Zener diode with the specification : Vz=9.3V, R_{se}=12.5 Ω

Transistor with specification I_C=100mA, β=100

DISCUSSION:

1. Which is the controlled element in the series and shunt voltage regulator and why.
2. Which element determines the output ripple?
3. Mention the applications of series voltage regulator?
4. What is meant by a constant-current limiting?
5. How the transistor is controls the output voltage.

EXPERIMENT -5

AIM:-Design a single stage FET amplifier with a voltage gain (A_V) = 102.5, lower cut off frequency of 100 Hz and upper cut off frequency of 1kHz. Plot the frequency response of the amplifier.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board (+12V & -12V)

COMPONENT REQUIRED:-

Capacitors and resistors of desired values, FET.

THEORY:

FET amplifier provide an excellent voltage gain with the added feature of a high input impedance. They are also low power consumption configurations with good frequency range. The device can amplify analog or digital signals. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the *drain*. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the *gate*. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET*).* The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification,

such as is required in large wireless communications and broadcast transmitters. Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain thousands of FETs, along with other components such as resistors, capacitors, and diodes.

CIRCUIT DIAGRAM:-

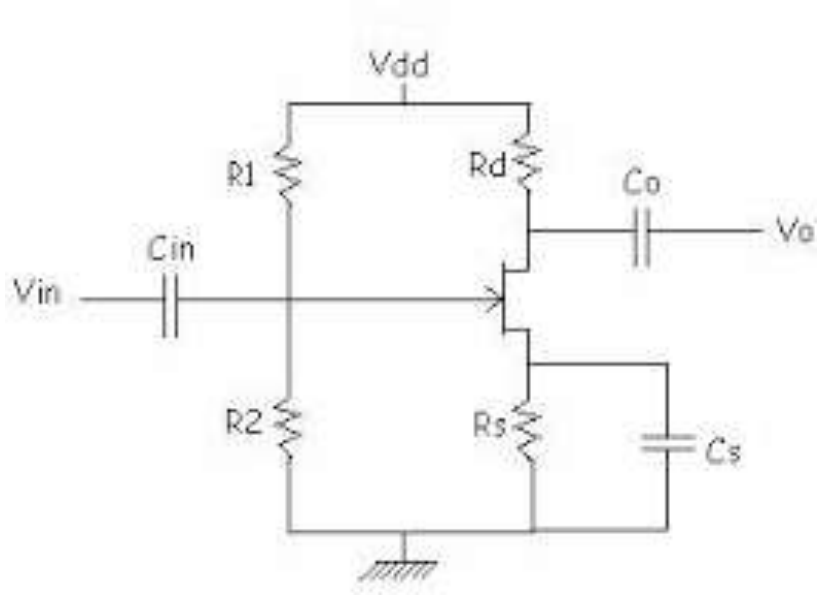


Fig. 5.1: FET Amplifier

DESIGN PROCEDURE:

Given: Amplifier gain (A_V)=102.5

Let I_{DSS}= 15mA, V_P= - 4V, C_S=1µF ,V_{DD}=9V

$g_{mo} = \frac{-2I_{DSS}}{V_P}$ => $\frac{-2\times15\times10^{-3}}{-4}$ =>7.5

Let V_{GS}=-2V

$g_m = g_{mo}(1 - \frac{V_{GS}}{V_P})$ =>7.5 (1- ($\frac{-2}{-4}$)) => 3.75

A_V= 102.5V

A_V = - $g_m R_D$

-($3.75\times10^{-3}R_D$)= 10.125

R_D= 2.7kΩ

R_{in}=R_G=2MΩ (Because FET has high input impedance)

$i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right) => 15\times10^{-3}\left(1 - \left(\frac{-2}{-4}\right)\right) => 22.5 \times 10^{-3}$

$V_{in} = V_{GS} + i_D R_S$

$500\times10^{-3} = (-2) + 22.5\times10^{-3} R_S$

$R_S = 111.1\Omega$

Find out the values of coupling capacitors C_{in} & C_{out} from given values of lower cut off frequency and upper cut off frequency.

$$f_L = \frac{1}{2\pi(R_G + R_{Signal})C_{in}}$$

$R_G >> R_{Signal}$

$$f_L = \frac{1}{2\pi R_G C_{in}} => 100 = \frac{1}{2\pi \times 2 \times 10^6 C_{in}}$$

$C_{in} = 7.95\times10^{-10} F$

$$f_L = \frac{1}{2\pi(R_{out} + R_L)C_o}$$

$R_{out} >> R_L$ and $R_{out} = R_D$

$$f_H = \frac{1}{2\pi R_D C_o} => 1000 = \frac{1}{2\pi \times 2.7 \times 10^3 C_o}$$

$C_o = 5.89\times10^{-8} F$

PROCEDURE:

1. To design an amplifier, find the value R_D from the given values of mid band gain $A_{v.}$
2. Next we have to calculate the value of R_S from V_{GS} & I_D.
3. Find out coupling capacitor values C_{in} & C_o by using lower cut off frequency(f_L) & upper cut off frequency(f_H).
4. Apply input to the circuit by using function generator.
5. Observe the output on CRO by varying the frequency of input signal from function generator.
6. Calculate gain in dB using given equation.
7. Plot the frequency response curve between gain and frequency.

OBSERVATION: Vin: 500mV

Table 5.1 Voltage gain variation with frequency

S.No.	Freq.	V_{out}(V)	Voltage Gain(V_o/V_i)	Voltage Gain in dB ($20 \log_{10} V_o/V_i$)
1	20 Hz			
2	50 Hz			
3	70 Hz			
4	100 Hz			
5	500 Hz			
6	1×10^3			
7	10×10^3			
8	100×10^3			
9	300×10^3			
10	500×10^3			
11	700×10^3			

Bandwidth=Upper cut of frequency (f_L)-Lower cut off frequency (f_H)

Model Graph

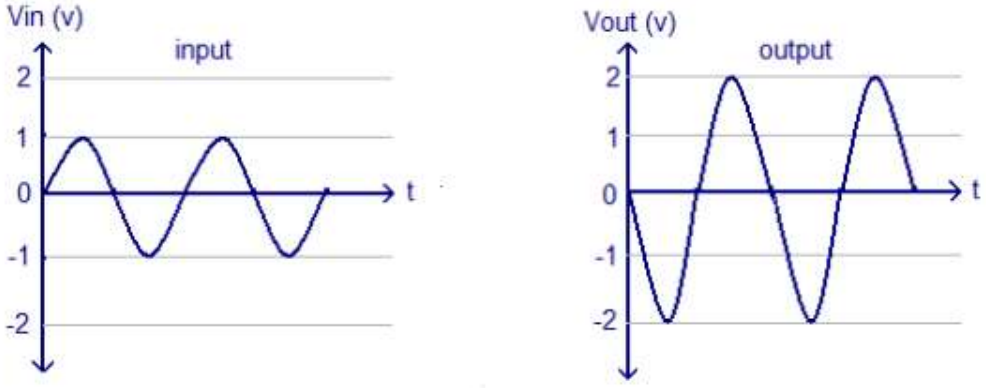


Fig. 5.2 Input and output waveform of the FET amplifier

FREQUENCY RESPONSE:

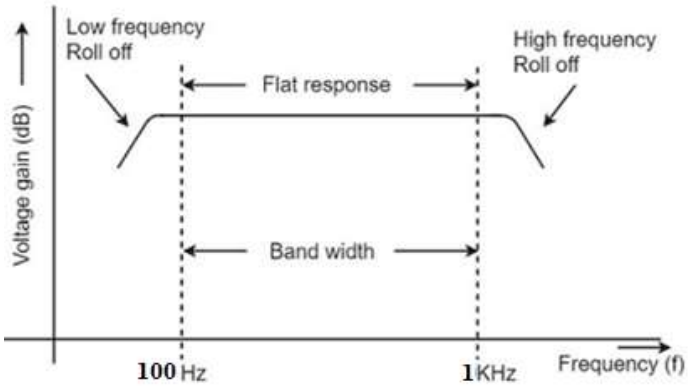


Fig. 5.2 Model graph and Frequency Resposne

RESULT:-

We have successfully designed a single stage FET amplifier with a voltage gain A_V = 102.5 and at a lower cut off frequency of 100Hz and upper cut off frequency of 1kHz.

Designed parameters are as follows:

R_D= 2.7kΩ, R_S = 111.1Ω, R_G=2MΩ, C_S=1μF, $C_{in} = 7.95 \times 10^{-10}$ F, C_o =5.89×10^{-8}F

We have plotted the frequency response curve for the designed amplifier. As per the frequency response curve, the gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. Thus Bandwidth is calculated with the help of upper and lower cut off frequency.

DISCUSSION:

1. What are the advantages of FET over BJT?
2. Mention the methods used for biasing circuits in FET.
3. Why MOSFET is called IGFET?
4. What is a drain current equation for a FET?
5. What is pinch off voltage in FET?

EXPERIMENT-6

AIM: Implementation of push pull amplifier and measure variation of output power & distortion with load and calculate the efficiency.

APPARATUS REQUIRED:

- Trainer Kit of Push Pull Amplifier model No:- Aditron (4521)
- CRO (Dual channel , 20 MHz)
- Function Generator (1MHz, 30Vpp)

THEORY:

The Class B configuration can provide better power output and has higher efficiency (up to 78.5%). The advantages of Class B push pull amplifiers are, ability to work in limited power supply conditions (due to the higher efficiency), absence of even harmonics in the output, simple circuitry when compared to the Class A configuration etc. The disadvantages are higher percentage of harmonic distortion when compared to the Class A, cancellation of power supply ripples is not as efficient as in Class A push pull amplifier and which results in the need of a well regulated power supply.The circuit diagram of a classic Class B push pull amplifier is shown in the diagram below.

The input signal is converted into two similar but phase opposite signals by the input transformer T1. One out of these two signals is applied to the base of the upper transistor while the other one is applied to the base of the other transistor. You can understand this from the circuit diagram. When transistor Q1 is driven to the positive side using the positive half of its input signal, the reverse happens in the transistor Q2. That means when the collector current of Q1 is going in the increasing direction, the collector current of Q2 goes in the decreasing direction. Anyway the current flow through the respective halves of the primary of the T2 will be in same direction. This current flow through the T2 primary results in a wave form induced across its secondary. The wave form induced across the secondary is similar to the original input signal but amplified in terms of magnitude.

Cross over distortion.

Cross over distortion is a type of distortion commonly seen in Class B amplifier configurations. Silicon transistor requires 0.7V and a Germanium diode requires 0.3V of voltage across its base emitter junction before entering in to conducting mode and this base emitter voltage is called cut in voltage. Germanium diodes are out of scope in amplifiers and used a Class B push pull amplifier based on Silicon transistors. Since the transistors are biased to cut off, the voltage across their base emitter junction remains zero during the zero input condition. The only source for the transistors to get the necessary cut in voltage is the input signal itself and the required cut in voltage will be looted from the input signal itself. As a result portions of the input wave form that are below 0.7V (cut in voltage) will be cancelled and so the corresponding portions will be absent in the output wave form too.

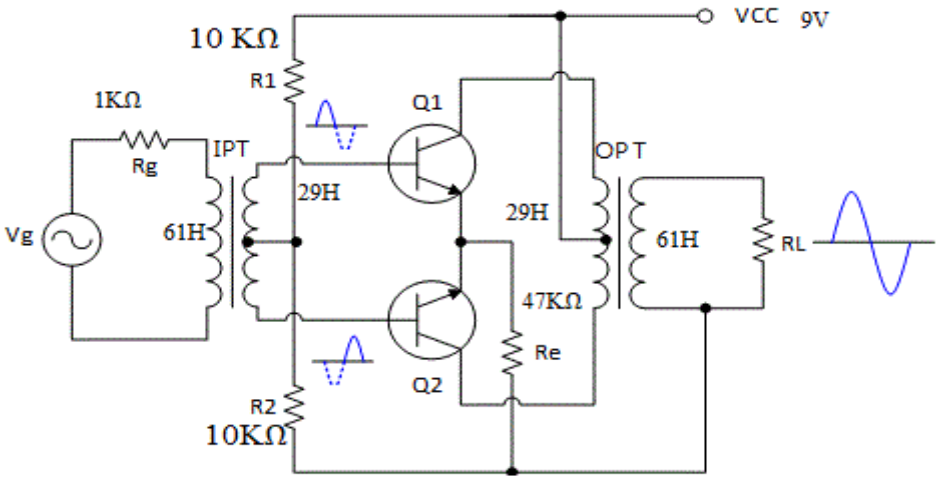


Fig. 6.1 Circuit diagram of push pull Amplifier

PROCEDURE:

I. Connect the DC supply (9 V) to the circuit (fig 6.1) from the source.

II. Apply sinusoidal signal of frequency ~1 kHz, amplitude 1V peak to peak to the Input of power amplifier.

III. Turn variable resistance R_L to observe the cross-over distortion. Trace it.

IV. Tune R_L in such a way so that the cross over distortion is removed (or brought to

Minimum. Trace it.

V. Record output voltage as a function of R_L in the range of few ohms to 200kΩ

VI. Plot the graph between load impedance (R_L) and output power (P_O).

VII. Find the maximum power for the optimum load. Calculate the % efficiency.

VIII. Replace R_L with a speaker at the output, across the secondary of output Transformer Tr2

IX. Try to hear the sound as a function of frequency and note down the frequency range for which the sound is audible.

OBSERVATION: Input Voltage:1 V and frequency :1KHz

Table 6.1 Output power variation with load resistance

S.No	Load Resistance R_L	Input Power Pi	Output voltage	Output power P_O	Efficiency $\eta=\frac{P_O}{P_i}X100$
1	50Ω				
2	100 Ω				
3	200 Ω				
4	1K Ω				
5	2 K Ω				
6	3 K Ω				
7	5 K Ω				
8	10 K Ω				
9	50 K Ω				
10	100 K Ω				

Calculations:

- Selected value of optimum load =
- Frequency of input signal =
- Maximum output power Po max =

At optimum Load : ……..

% efficiency $(\boldsymbol{\eta})=\frac{P_O}{P_i} X100$

P_O=output power

P_i =input power

RESULT: We have measured the variation of output power & distortion with load and calculate the efficiency

- Max. output power = ……
- Optimum load impedance = ……
- % efficiency = ……

DISCUSSION:

1. What is the harmonic distortion in power amplifier?
2. In class B power amplifiers why crossover distortion will be occurred?
3. What are the different methods to eliminate distortion?
4. How much efficiency will b obtained in class-B power amplifier?
5. Where is the location of operating point in class-B power amplifier?

EXPERIMENT-7

AIM: Design a Wein bridge oscillator for frequency f=1.6 KHz and observe the effect of variation in oscillator frequency.

APPARATUS REQUIRED:

- Trainer Kit of Wein Bridge Oscillator model No:- OMEGA(ETB94)
- CRO (Dual channel , 20 MHz)

COMPONENTS REQUIRED

Desired values of Capacitor and resistors

THEORY:

The Wein bridge oscillator is a standard circuit for generating low frequencies in the range of 10 Hz to about 1MHz.The method used for getting +ve feedback in wein bridge oscillator is to use two stages of an RC-coupled amplifier. Since one stage of the RC-coupled amplifier introduces a phase shift of 180 deg, two stages will introduces a phase shift of 360 deg. At the frequency of oscillations *f* the +ve feedback network shown in fig makes the input & output in the phase. The frequency of oscillations is given as

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

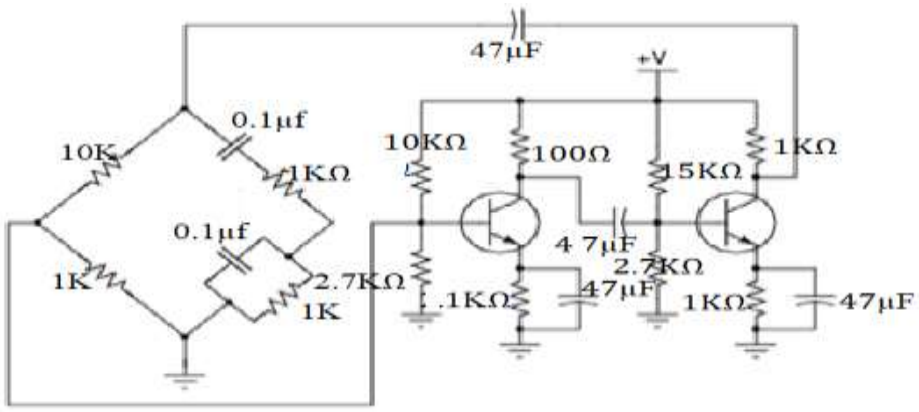


Fig 7.1: Circuit for wein bridge oscillator

DESIGN PROCUDURE:

The oscillator frequency is given by:

$$\mathbf{f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}}$$

if $R_1=R_2$ =R and $C_1=C_2$=C then oscillator frequency's=$\frac{1}{2\pi RC}$ and $R_3=2R_4$

Let us:$C=C_1=C_2$=0.1 µf and f=1600Hz

Then: $R_1=R_2=R=\frac{1}{2X\pi X1600\times0.1\times10^{-6}}$ =1KΩ

Let R_4=5 KΩ then R_3=10KΩ

PROCEDURE:

1. Make the connection as per the circuit diagram as shown above.
2. Observe the output signal and note down the output amplitude and time period (T_d).
3. Calculate the frequency of oscillations theoretically and verify it practically ($f=1/T_d$).

OBSERVATION:

Table 7.1 Oscillator frequency for different C and R

S.No	C	R	Theoretical frequency	Practical frequency	Error
1					
2					
3					

Model Wave Form:

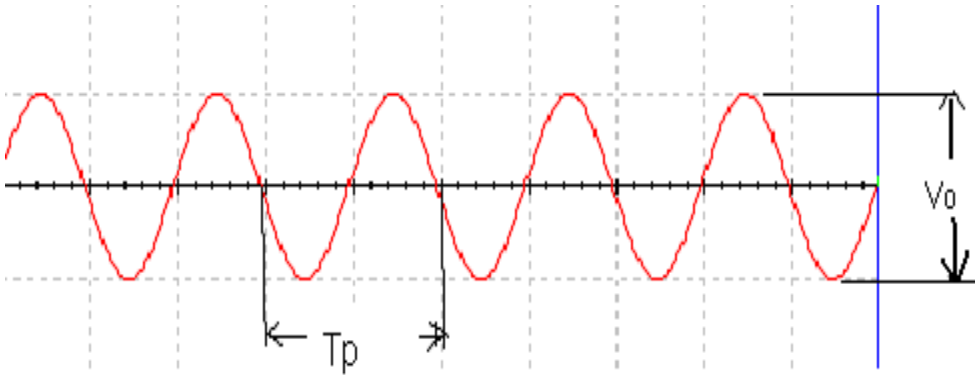


Fig 7.2: Output waveform of Wein Bridge oscillator

RESULT: We have successfully designed an Wein bridge oscillator of a frequency 8 kHz. Designed parameters are as follows:

$C=C_1=C_2=0.1$ µF, $R_1=R_2=R=1k\Omega$

We have also calculated the:

Theoretical frequency……..Hz,

Practical frequency……..Hz .

Percentage Error……..%

DISCUSSION:

1. What is the condition for wein bridge oscillator to generte oscillations?
2. What is the total phase shift provided by the oscillator?
3. What is the function of lead-lag network in Wein bridge oscillator?
4. Which type of feedback is used in Wein bridge oscillator?
5. What is the gain of Wein bridge oscillator?
6. What are the application of Wein bridge oscillator?
7. What is the difference between damped oscillations undamped Oscillations?

EXPERIMENT -8

AIM: Design a phase shift oscillator of frequency 650Hz and observe the effect of variation in R & C on oscillator frequency and compare with theoretical value.

APPARATUS REQUIRED:

1. Trainer Kit of Phase Shift Oscillator model No:- OMEGA(ETB94)
2. CRO (Dual channel , 20 MHz)

COMPONENTS REQUIRED

Desired values of Capacitor and resistors

THEORY:

RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feedback Networks the output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequencies. Since CE Amplifier produces 180 º phases shift the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than or equal to 1, this condition used to generate the sinusoidal oscillations.

The frequency of oscillations of RC-Phase Shift Oscillator is,

$$\mathbf{f} = \frac{1}{2\pi RC\sqrt{6}}$$

Circuit Diagram:

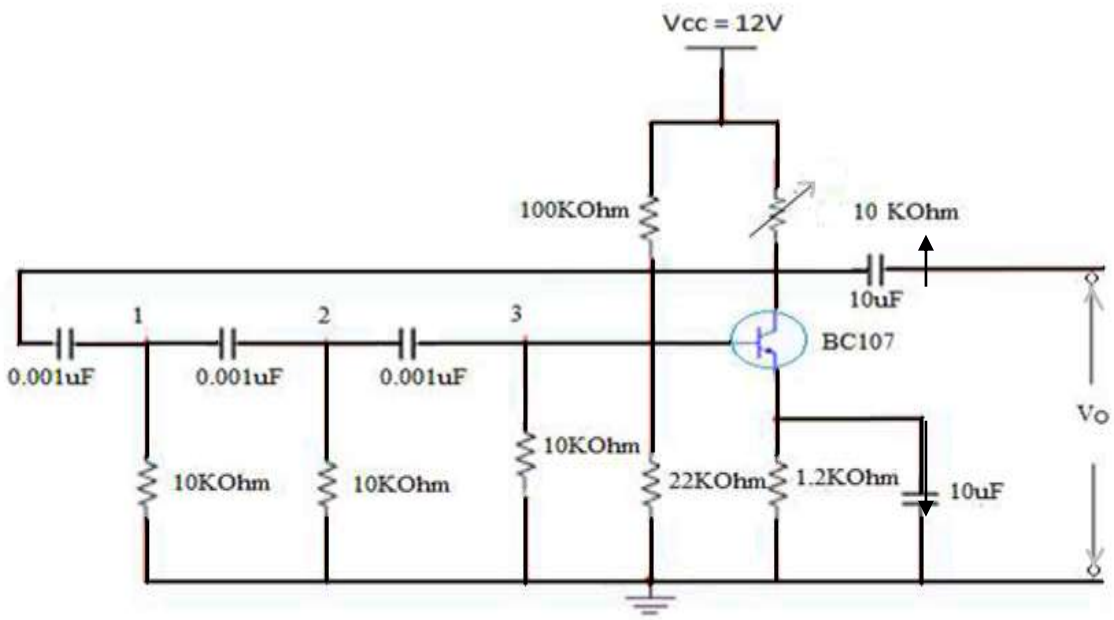


Fig 8.1: Circuit for RC Phase Shift Oscillator

Design Calculation:

Let us C = 0.001 uF .Given f=650Hz

The oscillator frequency is given by: $\mathbf{f = \frac{1}{2\pi RC\sqrt{6}}}$

$$R = \frac{1}{2 \times 3.14 \times 650 \times 0.001 \times 10^{-6}\sqrt{6}} = 10K\Omega$$

PROCEDURE:

I. Make the connection as per the circuit diagram as shown above.

II. Observe the output signal and note down the output amplitude and time period (T_d).

III. Calculate the frequency of oscillations theoretically and verify it practically ($f=1/T_d$).

IV. Calculate the phase shift at each RC section by measuring the time shifts (T_p) between the final waveform and the waveform at that section by using the below formula.

OBSERVATION TABLE:

S.No	C	R	Theoretical frequency	Practical frequency	Error
1					
2					
3					

Model Wave Forms:

Output Waveform:

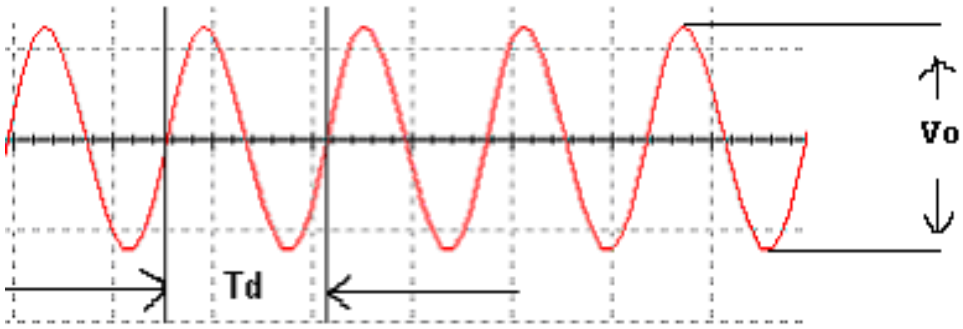


Fig 8.2: Output Waveform of RC Phase shift oscillator

RESULT: We have successfully designed an Phase shift oscillator of a frequency 650 Hz. Designed parameters are as follows:

C = 0.001 uF, R=10kΩ.

We have also calculated the:

Theoretical frequency……..Hz,

Practical frequency……..Hz .

Percentage Error……..%

DISCUSSION:

1. What are the conditions of oscillations?
2. Give the formula for frequency of oscillations?
3. What is the total phase shift produce by the RC ladder network?
4. Whether the oscillator is positive feedback or negative feedback?
5. What are the types of oscillator?

EXPERIMENT-9

AIM: (a) Design the Hartley oscillators of frequency 1.6 KHz and observe the effect of variation of capacitance on oscillator frequency.

(b) Design the Colpitts oscillators of frequency 2.25KHZ and observe the effect of variation of capacitance on oscillator frequency

APPARATUS REQUIRED:

- Trainer Kit of Hartley & Colpitt Oscillator model No:- OMEGA(ETB94)
- CRO (Dual channel , 20 MHz)

COMPONENTS REQUIRED

Desired values of Capacitor, Inductor and resistors

THEORY:

Hartley Oscillator:

The tank circuit shown in the circuit consist of two coils L1 & L2. The coil L1 is inductively coupled to the coil L2 and the combination work as an auto transformer. The feedback b/w the o/p & i/p circuits are accomplished through auto transformer action which also introduced a phase shift of 180^0 .The phase reversed b/w the o/p & i/p voltages occur because they are taken from the opposite ends of the coils (L1 & L2) with respect to the tap which is grounded. The frequency of oscillator is given by

$$\mathbf{f=\frac{1}{2\pi\sqrt{C(L_1+L_2+2M)}}}$$

Where L_1=Inductance of primary coil

L_2=Inductance of secondary coil

M=Mutual inductance between primary and secondary coil

C=Tank circuit capacitance

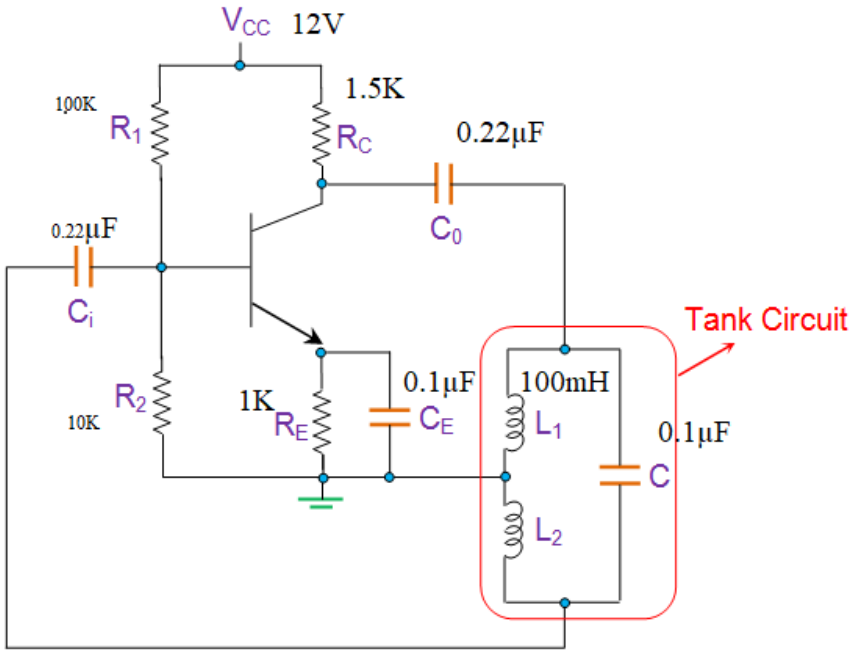


Fig 9.1. Hartley oscillator

Colpitts Oscillator:

Colpitts oscillator is a radio frequency oscillator which generates a frequency of the range of (30 KHz to 30MHz).The collector supply voltage VCC is applied to the collector transistor RC parallel combination of RE = CE with resistor R1 = R2 provides the stabilized self bias. The tuned circuit consists of C1, C2 & L are extending from collector act to the base act determines basically the transistor of oscillator. The feedback is through the tank circuit itself. The frequency of oscillator is given by

$$F_0 = 1/ 2\pi\sqrt{LC_{eq}}$$

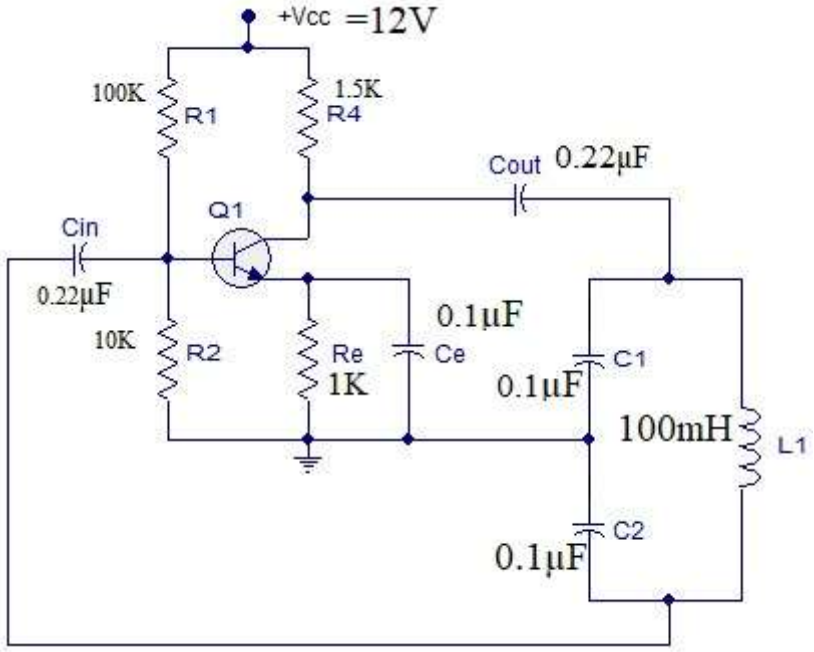


Fig 9.2: Colpitts Oscillator

$$\mathbf{f=\frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)}}}$$

Where L=Tank circuit inductance

C_1=Tank circuit capacitance

C_2=Tank circuit capacitance

DESIGN PROCEDURE:

Hartley Oscillator

Resonant or oscillation frequency is given by:$f=\frac{1}{2\pi\sqrt{C(L_1+L_2+2M)}}$

If L1+ L2=100mH ,M= 0 and f=1.6KHz

$$C=\frac{1}{4f^2\pi^2(L_1+L_2+2M)}$$

$$C=\frac{1}{4\,X1600X1600X3.14X3.14X100X10^{-3}}=0.1\mu F$$

Colpitts Oscillator:

Resonant or oscillation frequency is given by:$f=\frac{1}{2\pi\sqrt{L(\frac{C_1C_2}{C_1+C_2})}}$

If f=2250Hz , C1= 0.1µF , C2= 0.1µF

$$L=\frac{1}{4f^2\pi^2\frac{C_1C_2}{C_1+C_2}}$$

$$L=\frac{1}{4\times2250^2\times3.14^2\times\frac{0.1\times0.1\times10^{-12}}{0.2\times10^{-6}}}=100\text{mH}$$

PROCEDURE:

I. Design the tank circuit for the desired frequency.

II. Set the values of inductor and capacitor so as to get the required frequency of

III. Oscillation.

IV. Make the connections as shown in the circuit diagram.

V. Compare the values of theoretical and practical values of frequency.

OBSERVATION:

Table 9.1: Hartley oscillator.

Capacitance(uF)	Inductance(uH)			Frequency(Hz)			Percentage error
C	L1	L2	Leq=L1+L2	Time period T	Practical Value *F=1/T*	Theoretical **f=** $\frac{1}{2\sqrt{C(L_1+L_2+2M)}}$	

Table 9.2: Colpitts oscillator

Inductance(uH) L	Capacitance(uF)			Frequency(Hz)			Percentage error
	C1	C2	**C**eq= C1 C2/ C1+ C2	Time period T	Practical Value *F=1/T*	Theoretical $\mathbf{f=\frac{1}{2\sqrt{CeqL}}}$	

RESULT: We have successfully designed an Hartley and Colpitts oscillator of a frequency 8 kHz. Designed parameters are as follows:

For Hartley oscillator.

L1+ L2=100mH ,M= 0, f=1.6KHz and C=0.1µF

For Colpitts oscillator.

f=2250Hz , C1= 0.1µF , C2= 0.1µF and L=100mH

We have also calculated the Percentage Error in Theoretical frequency and Practical frequency.

DISCUSSION:

1. What is its need of oscillators?
2. Application of Hartley and Colpitts oscillator?
3. What are the conditions for oscillations?
4. What is the difference between Hartley and Colpitt's oscillators?
5. Why is amplifier circuit necessary in an oscillator?
6. How you will get undamped oscillations from a tank circuit?

EXPERIMENT-10

AIM: Design a non-inverting amplifier for A_f (gain with feedback) = 10 and an inverting amplifier for A_f (gain with feedback) = -10 using op-amp 741.

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APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board (+12V & -12V)

COMPONENT REQUIRED:-

Capacitor and resistors of desired values, Op-amp IC 741

THEORY:-

Op-amp can be connected to negative feedback to stabilize gain and increase the frequency response. The extremely high open loop gain of an op-amp creates an unstable situation because a small noise voltage on the input can be amplified to a point where the amplifier is driven out of its linear region. The open loop gain parameter of an op-amp can vary greatly from one device to the other. Negative feedback takes the portion of output and applies it back to the input, creating effective reduction in gain. This closed loop gain is usually much less than the open loop gain.

Non-Inverting Amplifier:-

In case of non-inverting amplifier, the input is applied to the non-inverting input. The output and input are in phase. The input resistance of an inverting amplifier is smaller as it depends on the series resistance connected to the input- signal-source.

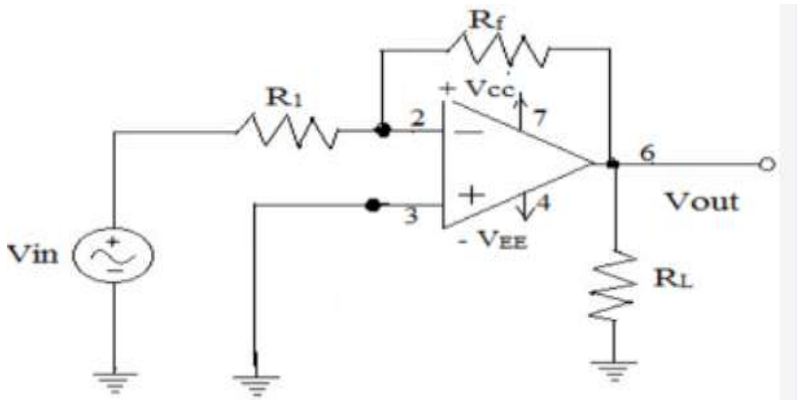

Fig.10.1 Non-inverting amplifier

This differential voltage is amplified by the gain of the op-amp and produces an output voltage expressed as

$$V_o = (1 + \frac{R_F}{R_1})V_{in}$$

Inverting Amplifier:-

In inverting amplifier configuration the input is given to the inverting terminal, hence the output obtained is inverted, i.e. 180 degrees out of phase with the applied input. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted.

The Inverting operational amplifier gain can be expressed using the equation

$$V_O = -\frac{R_F}{R_i}V_{in}$$

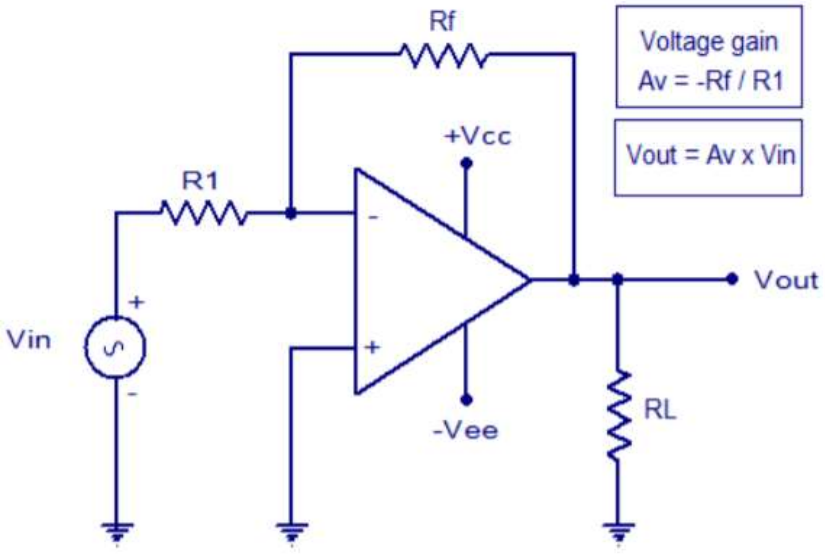

Fig.10.2 Inverting amplifier

DESIGN PROCEDURE:

(i) Non-inverting op-amp

Closed loop voltage gain is given by

$$A_f = 1 + \frac{R_f}{R_1}$$

Since we need to design a non-inverting amplifier for A_f (gain with feedback) = 10

So:

$$R_f / R_1 = 9$$

$$\text{So } R_f = 9R_1$$

Let $R_1 = 1k\Omega$, then $R_f = 9\ K\Omega$

(2)Inverting op-amp

Closed loop voltage gain is given by

$$A_f = -\frac{R_f}{R_1}$$

Since we need to design a non-inverting amplifier for A_f (gain with feedback) = -10

So:

$$-(R_f / R_1) = -10$$

$$\text{So } R_f = 10R_1$$

Let $R_1 = 470\Omega$, then $R_f = 4.7\ k\Omega$

PROCEDURE:

Procedure For Non-Inverting Amplifier With Feedback

- To achieve the desired gain we have to calculate the value of R_f and R_1
- Determine relation between R_1 and R_f from the given value of A_f.
- Calculate the value of R_f with the help of choosing value of R_1.
- Connect the circuit as shown in figure.
- Apply AC input signal from function generator on pin 3 of IC 741.
- Connect CRO at pin 6 of IC 741.
- Apply 1kHz frequency for ac input signal.
- Observe input and output waveform simultaneously on CRO in dual mode.

Procedure For Inverting Amplifier With Feedback

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- Determine relation between R_1 and R_f from the given value of A_f.
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- Apply AC input signal from function generator on pin 3 of IC 741.

- Connect CRO at pin 6 of IC 741.
- Apply 1kHz frequency for ac input signal.
- Observe input and output waveform simultaneously on CRO in dual mode.

OUTPUT WAVEFORM

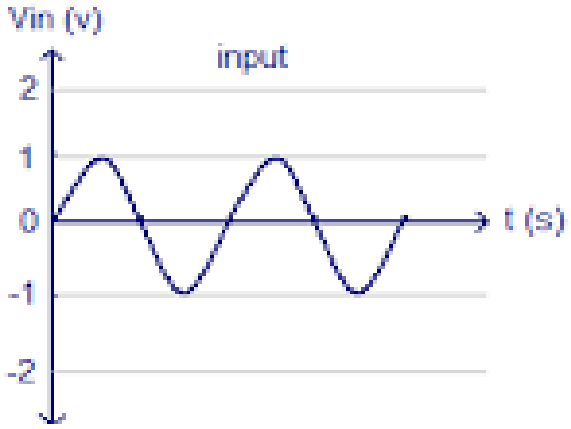

Fig. 10.3 Input waveform of Non-inverting amplifier

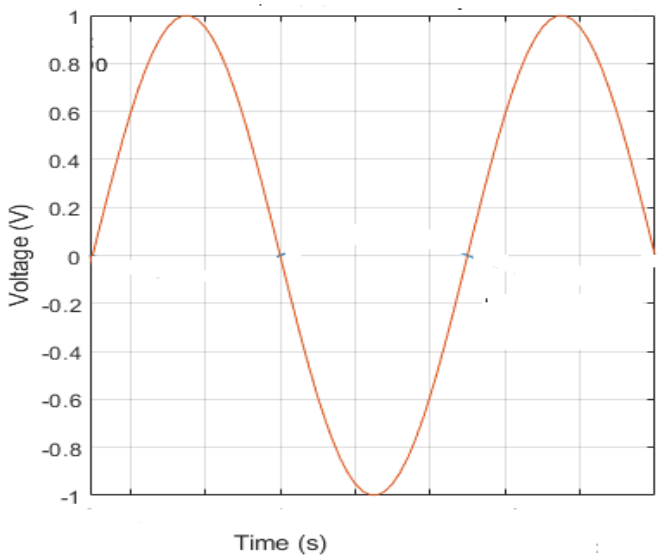

Fig. 10.4 Output waveform of Non-inverting amplifier

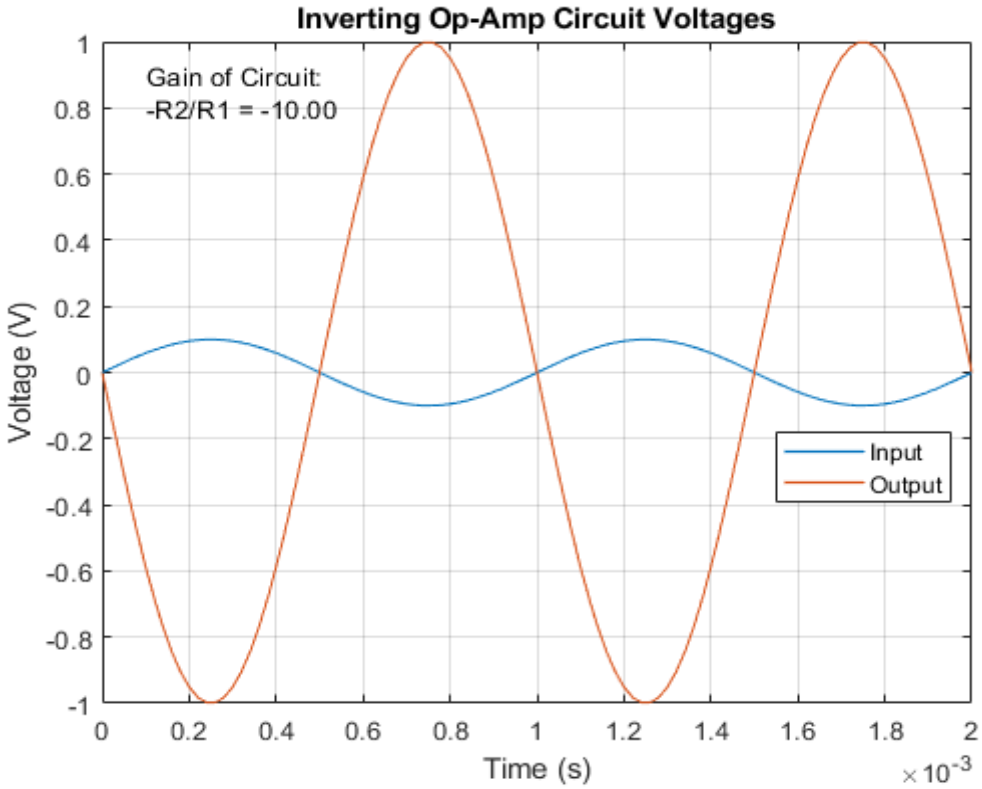

Fig. 10.5 Input and Output waveform of Inverting amplifier

RESULT:-

We have successfully designed a non-inverting amplifier for A_f (gain with feedback) = 10 and an inverting amplifier for A_f (gain with feedback) = (-10) using op-amp 741.

Designed parameters are as follows:

non-inverting amplifier: $A_f = 11$, R_1=1 kΩ, $R_f = 9$ kΩ

Inverting amplifier: AF = -10, $R_1 = 470$Ω, $R_f = 4.7$ kΩ.

We have obtained 180° and 0° phase shift in inverting and non-inverting amplifier respectively.

DISCUSSION:

1. What is the difference between inverting and non-inverting amplifier?
2. Which feedback topology is called inverting amplifier.
3. How gain of non-inverting amplifier can be changed.
4. How is the gain depends on feedback resistance .
5. What is the concept of virtual ground in op-amp?

EXPERIMENT-11

AIM:-

(a) Design a summing amplifier circuit in which the output must be equal to two times the negative sum of the inputs of Operational Amplifier.

(b) Design a Scaling amplifier circuit that will amplify the first input by a factor of 4, second by a factor of 2 and third by a factor of 1 of Operational Amplifier.

(c) Design an Averaging circuit for three DC inputs of Operational Amplifier.

APPARATUS REQUIRED:-

- Function generator
- Multi-metrer
- Bread board with power supply (±12V).
- Three variable DC power supply

COMPONENT REQUIRED:-

OPAMP IC 741, and resistors of desired values

THEORY:

Summing Amplifier: Op-amp may be used to perform the summing operation of several input signals in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively.

The summing amplifier is used for combining several signals. The most common use of a summing amplifier with two inputs is the amplification of signal combined with a subtraction of a constant amount from it(dc offset).

The output voltage, (Vout) now becomes proportional to the sum of the input voltages, V_1, V_2, V_3 etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus

The Summing Amplifier is a very flexible circuit indeed, enabling us to effectively "Add" or "Sum" together several individual input signals. However, if the input resistors

are of different values a "scaling summing amplifier" is produced which gives a weighted sum of the input signals.

Scaling amplifier : In a scaling amplifier each input will be multiplied by a different factor and then summed together. Scaling amplifier is also called a weighted amplifier. Here different values are chosen for R_1, R_2 and R_3.

Averaging of Operational Amplifier

An averaging amplifier circuit in which the output voltage is equal to the negative average of all the input voltage applied at the inverting terminal of op-amp. This can be accomplished by using input resistance R_1 & R_2 and R_3 of equal value and three times of R_F i.e.

If in the circuit $=R_1=R_2=R_3=3R_F$,

$$V_0=-(\frac{V_1+V_2+V_3}{3})$$

DESIGN PROCEDURE:

Design Calculation for summing amplifier:

Let us consider R_{in}=1.8KΩ, R_F=3.6 KΩ

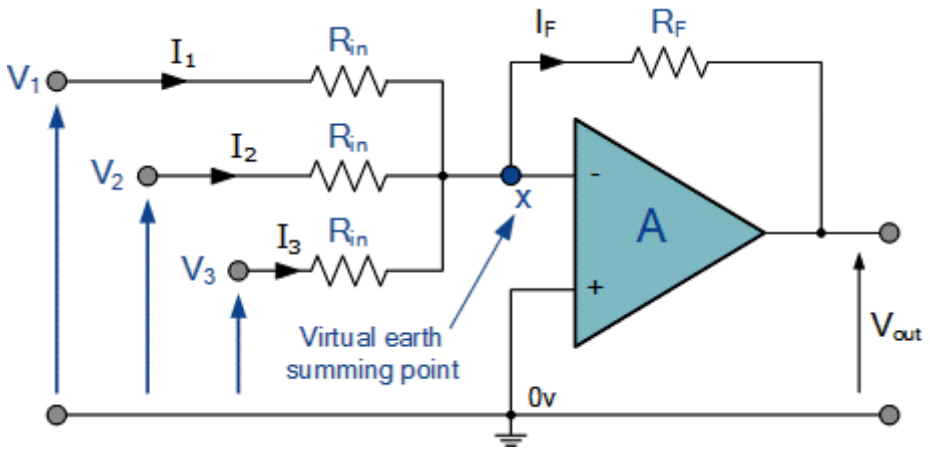

Fig. 11.1 Circuit diagram of summing amplifier

Apply the KCL at Node X

$$\frac{V_1}{R_{in}}+\frac{V_2}{R_{in}}+\frac{V_3}{R_{in}}=\frac{0-V_{out}}{R_F}$$

$$Vout=-\frac{R_F}{R_{in}}(V_1+V_2+V_3)\ldots\ldots\ldots\ldots\ldots(1)$$

Put the given values

$$V_{out}=-\frac{3.6}{1.8}(V_1+V_2+V_3)$$

$$V_{out} = -2(V_1 + V_2 + V_3)$$

Design Calculation for scaling amplifier:

Let us consider: R_1=1 KΩ, R_F=4 KΩ, R_2=2 KΩ, R_3=4 KΩ

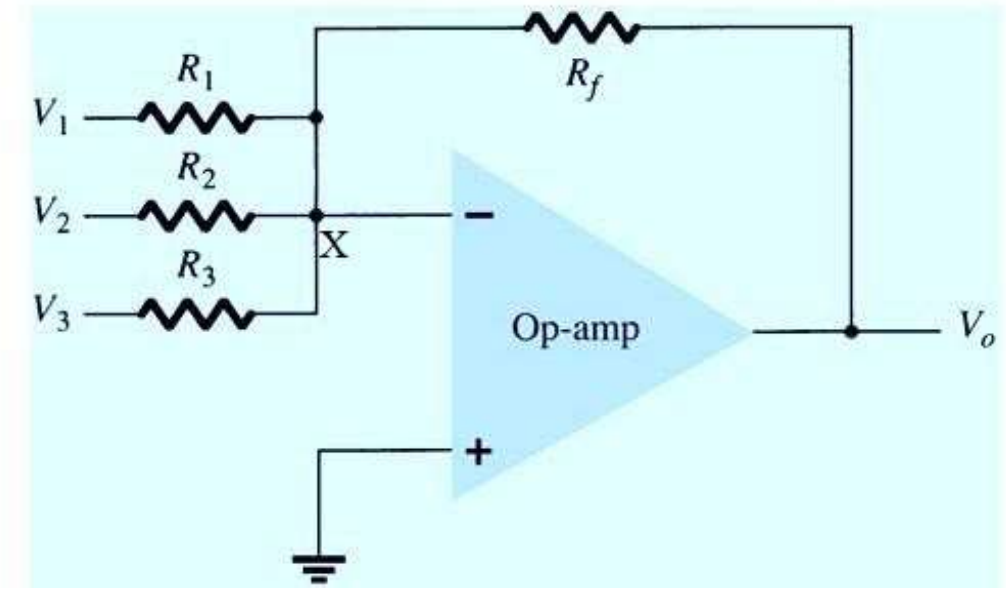

Fig.11.2 Scalar amplifier in inverting mode

The scalar amplifier in inverting mode is shown in fig.3.1 The transfer function of the scalar amplifier is

Apply the KCL at Node X

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{0 - V_o}{R_F}$$

$$V_o = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right) \ldots\ldots\ldots\ldots (2)$$

The condition is: $\frac{R_F}{R_1} \neq \frac{R_F}{R_2} \neq \frac{R_F}{R_3}$

Putting the given values:

$$V_o = -(4V_1 + 2V_2 + V_3)$$

Design Calculation for averaging amplifier:

From equation (2) $R_1 = R_2 = R_3 = 3R_F$,

$$V_0 = -\left(\frac{V_1 + V_2 + V_3}{3}\right) \ldots\ldots\ldots\ldots (3)$$

This means that the output voltage is the negative average of three input voltages hence it is called as averaging amplifier.

Circuit diagram of Average amplifier:

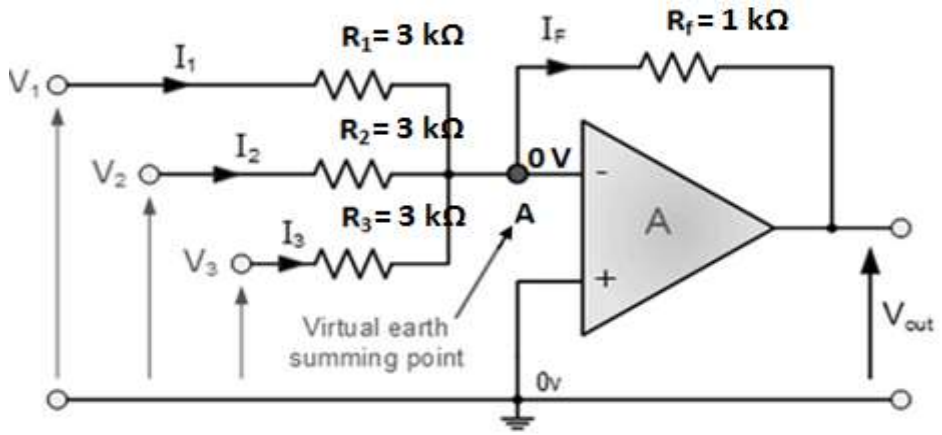

Fig.11.3 Circuit diagram of Average amplifier

PROCEDURE:-

11(a)Procedure for summer

- Connect the circuit as shown in fig.11.1.
- Apply DC input signal of three different values and measure output through multimeter at output terminal.
- Compare theoretical & practical output values.

11(b) Procedure For Scalar

- Connect the circuit as shown in fig.11.2 of scalar or weighted amplifier in inverting mode.
- Apply DC input signal of three different values and measure output through multimeter at output terminal.
- Compare theoretical & practical output values.

11(c)Procedure for Average amplifier

- Connect the circuit as shown in fig.11.3.
- Apply DC input signal of two different values and measure output through multimeter at output terminal.
- Compare theoretical & practical output values.

OBSERVATIONS:-

Table 11.1: Summing amplifier in inverting mode

S.NO.	V_1	V_2	V_3	(Practical)	(Theoretical) $V_{out} = -2(V_1 + V_2 + V_3)$
1					
2					
3					
4					
5					

Table 11.2: Scalar or weighted amplifier in inverting mode

S.NO.	V_1	V_2	V_3	(Practical) Vo	(Theoretical) $Vo=-(4V_1+2V_2+V_3)$
1					
2					
3					
4					
5					

Table 11.3 Average amplifier in inverting mode

S.NO.	V_1	V_2	V_3	(Practical)	(Theoretical) $V_0=-(\frac{V_1+V_2+V_3}{3})$
1					
2					
3					

RESULT:-

We have successfully designed the op-amp as:

(a). A summing amplifier circuit in which the output must be equal to two times the negative sum of the inputs and the practical values verified by theoretical value.

(b). A Scaling amplifier circuit that will amplify the first input by a factor of 4, second by a factor of 2 and third by a factor of 1 and the practical values verified by theoretical value.

(c). An Averaging circuit for three DC inputs and the practical values verified by theoretical value.

DISCUSSION-

1. How can you change the scale factor of the scalar circuit?
2. What is a virtual ground concept?
3. How does a virtual ground concept help to determine the output voltage in the case of scalar and summer application of op-amp?
4. Is there any limitation of scalar and summer circuit?
5. In what way is the voltage follower a special case of the non-inverting amplifier?

EXPERIMENT-12A

AIM:-

Design a first order low pass filter at a cutoff frequency of 1 kHz with a pass band gain of 6 dB. using op-amp 741.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board (+12V & -12V)

COMPONENT REQUIRED:-

Capacitor and resistors of desired values, Op-amp IC 741

THEORY:-

A low-pass filter (LPF) is a filter that passes signals with a frequency lower than a selected cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency.

RC Passive Filter (low pass filter) can be made using a single resistor in series with a capacitor connected across a sinusoidal input signal. The main disadvantage of passive filters is that the amplitude of the output signal is less than that of the input signal, i.e. the gain is never greater than unity and that the load impedance affects the filters characteristics.

With passive filter circuits containing multiple stages, this loss in signal amplitude called "Attenuation" can become quiet severe. One way of restoring or controlling this loss of signal is by using amplification through the use of **Active Filters**.

As their name implies, **Active Filters** contain active components such as operational amplifiers, transistors or FET's within their circuit design.

A first-order low pass filter has the same magnitude and phase response characteristics as a passive RC filter with the exception of the fact that you can have gain in the pass band.

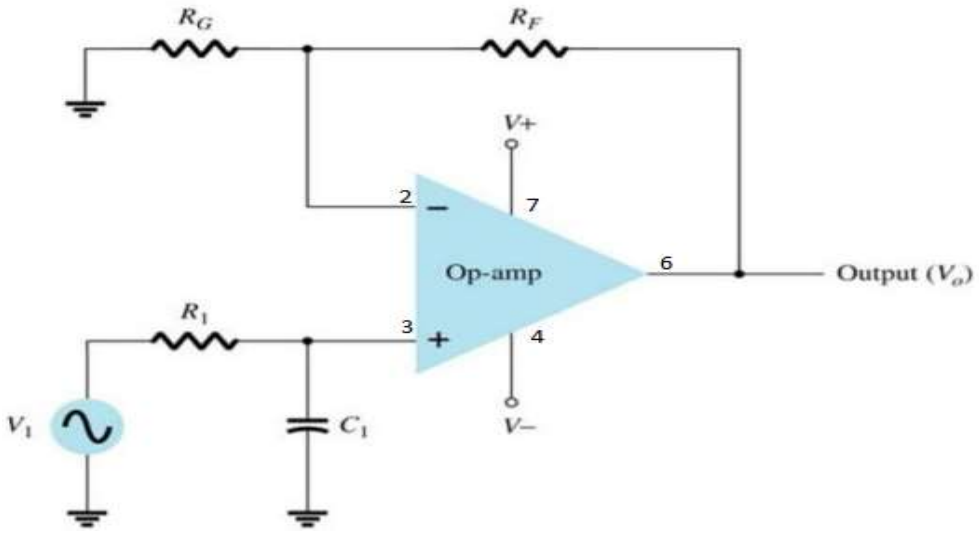

Fig 12.1. Circuit diagram of low pass filter

This low pass filter consists of two sections: The first is a passive low pass filter (using capacitor C_1 and resistor R_1). The second is a non–inverting op-amp.

Voltage Gain of a first-order low pass filter

Voltage gain can be given by the expression as:

$$\frac{V_{out}}{V_{in}} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}}$$

Where:

- A_F = the pass band gain of the filter, $(1 + R_F/R_G)$
- f = the frequency of the input signal in Hertz, (Hz)
- f_c = the cut-off frequency in Hertz, (Hz) and can be defined by the expression

$$f_c = \frac{1}{2\pi R1C1}$$

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as-

1. At very low frequencies, $f < fc$

$$\frac{Vout}{Vin} = A_F$$

2. At the cut-off frequency, $f = fc$

$$\frac{\text{Vout}}{\text{Vin}} = \frac{\text{AF}}{\sqrt{2}} = 0.707\ A_F$$

3. At very high frequencies, $f > fc$

$$\frac{\text{Vout}}{\text{Vin}} < A_F$$

Thus, the Active Low Pass Filter has a constant gain A_F from 0 Hz to the high frequency cut-off point, f_C. At f_C the gain is $0.707A_F$, and after f_C it decreases at a constant rate as the frequency increases. That is, when the frequency is increased tenfold (one decade), the voltage gain is divided by 10.

In other words, the gain decreases 20dB (= 20*log(10)) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

Voltage Gain in (dB)

$$A_v(\text{dB}) = 20 \log_{10} \left(\frac{\mathbf{Vout}}{\mathbf{Vin}}\right)$$

$$\left(\frac{\mathbf{Vout}}{\mathbf{Vin}}\right) = A_f = 1 + \frac{\boldsymbol{Rf}}{\mathbf{RG}}$$

DESIGN PROCEDURE:

Cutoff frequency of a low pass filter is given by

$$f_c = \frac{1}{2\pi R1C1}$$

Since we need to design a filter with cut off frequency of 1 KHz i.e. f_c= 1 kHz

Let C_1= 0.01µf

$$R_1 = \frac{1}{2\pi fcC1}$$

By putting the value of f_c, and C_1, determine R_1

$$R_1 = 15.9\ k\Omega.$$

Since pass band gain = 6 dB

So $20 \log A_f = 6$

$A_f = 2$

$A_f = 1 + \frac{Rf}{RG}$

So $R_f = R_G$

Let R_f =10 kΩ. so R_G=10 kΩ

PROCEDURE:

- To achieve the desired gain we have to calculate the value of A_f
- Calculate the value of R_G and R_f from the calculated value of $A_{f.}$
- Calculate the value of $R_1/C_1$with the help of desired cut off frequency f_c using given equation. First assume any value of C_1/R_1 for this.
- Connect the circuit as shown in figure.
- Apply AC input signal on pin 3 of IC 741.
- Observe the output on CRO by varying the frequency of input signal from function generator.
- Calculate gain in dB using given equation.
- Plot the frequency response curve between gain and frequency.
- Obtain the 3dB point for the frequency response curve.

OBSERVATION:-

Table 12.1 Gain with frequency

S.No.	Frequency (Hz)	V_{in}(V)	V_{out}(V)	A_v= 20 log (V_{out}/V_{in}) (dB)
1				
2				
3				
4				
5				
6				
7				

FREQUENCY RESPONSE CURVE

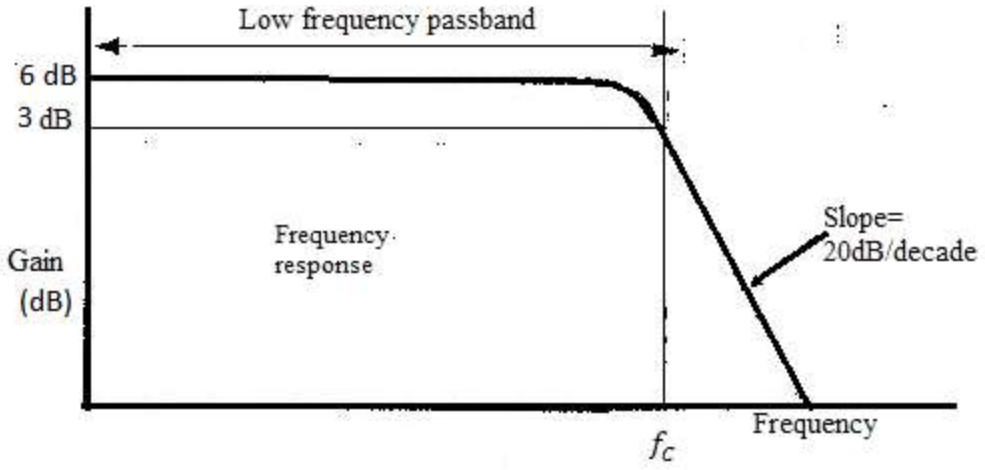

Fig 12.2. Frequency response of Low pass filter

RESULT:-

We have successfully designed a low pass filter of cut-off frequency 1 kHz with a pass band gain of 6 dB, using op-amp 741.

Designed parameters are as follows:

f_c= 1 kHz, A_f= 6dB, C_1 = 0.01µf, R_1=15.9 kΩ, , $R_f = R_G$

We have plotted the frequency response curve for the designed filter. As per the frequency response curve, the output voltage is constant for low frequencies till 1 kHz and then decreases with frequency. Further, we observed that gain is also constant for lower frequencies up to 1 kHz and decreasing for higher frequencies.

DISCUSSION:-

1. What do you mean by filter ? Why we required filter circuit?
2. Compare active and passive filters.
3. Draw the frequency response curve for low pass filter. Analyze different points on the curve.
4. What are the limitations of the low pass filter?
5. What is the significance of 3 dB gain in low pass filter?
6. What is the roll off rate of filter? How this rate can be varied?

EXPERIMENT-12 B

AIM:-

Design a first order high pass filter at a cutoff frequency of 1 kHz with a pass band gain of 6 dB. using op-amp 741.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board (+12V & -12V)

COMPONENT REQUIRED:-

Capacitor and resistors of desired values, Op-amp IC 741

THEORY:-

HIGH PASS FILTER

A high-pass filter (HPF) is a filter that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency.

The basic operation of a High Pass Filter (HPF) is exactly the same as that for its equivalent RC passive filter circuit, except that this type of circuit has an operational amplifier included within its design for amplification and gain control.

A 1^{st} order High Pass Active Filter as its name implies, attenuates low frequencies at the roll of rate of 20dB/Decade and passes high frequency signals. It consists simply a passive filter section which is having one pair of RC component followed by a non-inverting operational amplifier.

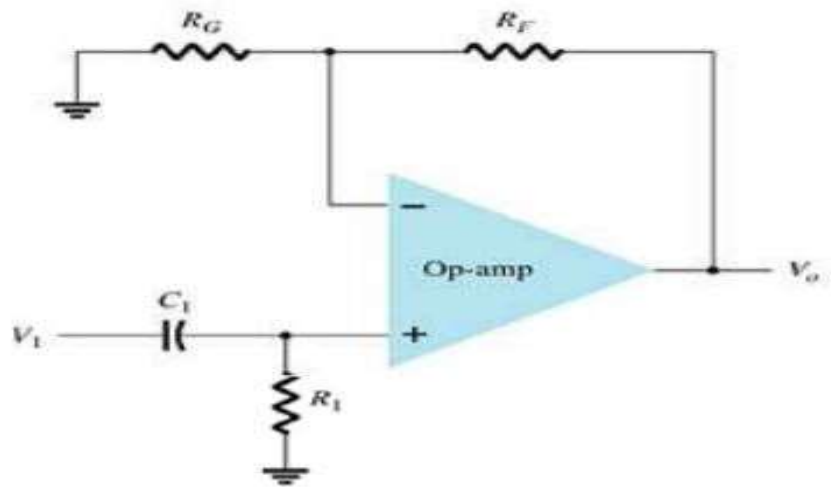

Fig 12.3. Circuit diagram of low pass filter

Voltage Gain of a first-order High pass filter

Voltage gain can be given by the expression as:

$$\frac{V_{out}}{V_{in}} = \frac{A_F}{\sqrt{1 + \left(\frac{f_c}{f}\right)^2}}$$

Where:

- A_F = the pass band gain of the filter, $(1 + R_F/R_G)$
- f = the frequency of the input signal in Hertz, (Hz)
- f_c = the cut-off frequency in Hertz, (Hz) and can be defined by the expression

$$f_c = \frac{1}{2\pi R1C1}$$

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as-

At very low frequencies, $f < fc$

$$\frac{Vout}{Vin} < A_F$$

At the cut-off frequency, $f = fc$

$$\frac{\text{Vout}}{\text{Vin}} = \frac{\text{AF}}{\sqrt{2}} = 0.707\ A_F$$

At very high frequencies, $f > fc$

$$\frac{\text{Vout}}{\text{Vin}} = A_F$$

Thus, the **Active Low Pass Filter** has a constant gain A_F for very high frequencies, At f_C the gain is $0.707A_F$, and from 0 Hz to lower cut-off point, f_C gain increases as frequency increases. That is, when the frequency is increased tenfold (one decade), the voltage gain is become 10 time.

In other words, the gain increases 20dB (= 20*log(10)) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

Voltage Gain in (dB)

$$A_v(\text{dB}) = 20 \log_{10} \left(\frac{\mathbf{Vout}}{\mathbf{Vin}}\right)$$

$$\left(\frac{\mathbf{Vout}}{\mathbf{Vin}}\right) = A_f = 1 + \frac{\boldsymbol{Rf}}{\mathbf{RG}}$$

DESIGN PROCEDURE:

Cutoff frequency of a low pass filter is given by

$$f_c = \frac{1}{2\pi R1 C1}$$

Since we need to design a filter with cut off frequency of 1 KHz i.e. f_c= 1 kHz

Let C_1= 0.01µf

$$R_1 = \frac{1}{2\pi f c C1}$$

By putting the value of f_c, and C_1, determine R_1

$$R_1 = 15.9\ k\Omega.$$

Since pass band gain = 12 dB

So 20 log A_f = 12

A_f = 4

$$A_f = 1 + \frac{Rf}{RG}$$

So $R_f = 3\ R_G$

Let R_G=10 kΩ so R_f =30 kΩ.

PROCEDURE:

- Calculate the value of R_1/C_1 with the help of desired cut off frequency f_c using given equation. First assume any value of C_1/R_1 for this.
- To achieve the desired gain we have to calculate the value of A_f
- Calculate the value of R_G and R_f from the calculated value of A_f.
- Connect the circuit as shown in figure 2
- Apply AC input signal on pin 3 of IC 741.
- Observe the output on CRO by varying the frequency of input signal from function generator.
- Calculate gain in dB using given equation.
- Plot the frequency response curve between gain and frequency.
- Obtain the 3dB point for the frequency response curve.

OBSERVATION:-

Table 12.2 Gain with frequency

S.No.	Frequency (Hz)	V_{in}(V)	V_{out}(V)	$A_v = 20 \log (V_{out}/V_{in})$ (dB)
1				
2				
3				
4				
5				
6				
7				

FREQUENCY RESPONSE CURVE

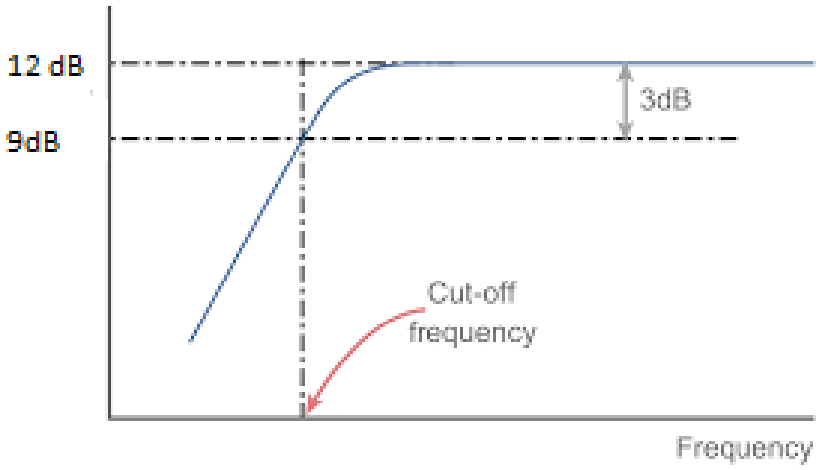

Fig 12.4. Frequency response of Low pass filter

RESULT:-

We have successfully designed a high pass filter of cut-off frequency 1 kHz with a pass band gain of 6 dB, using op-amp 741.

Designed parameters are as follows:

f_c= 1 kHz, A_f= 6dB, C_1 = 0.01µf, R_1=15.9 kΩ, , $R_f = 3R_G$

We have plotted the frequency response curve for the designed filter. As per the frequency response curve, the output voltage is decreases with frequency till high frequencies and constant after 1 kHz. Further, we observed that gain is decreasing for lower frequencies upto 1kHz and constant constant after 1 kHz.

DISCUSSION:-

1. What is meant by 3dB frequency.?
2. Draw the frequency response curve for high pass filter. Analyze different points on the curve.
3. What are the limitations of the high pass filter?
4. Why are active filers preferred.

Beyond Curriculum Experiment

EXPERIMENT-13

AIM:- Design an integrator circuit using Op-Amp for a desired frequency.

APPARATUS REQUIRED:-

- Function generator
- CRO
- Power Supply with Bread Board ((+12V & -12V)

COMPONENT REQUIRED:-

Capacitors and resistors of desired values, Op-Amp (IC 741).

THEORY:

Integrator:

A circuit in which the output voltage is the integration of the input voltage is called as the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f The expression for the output voltage Vo can be written as Recall that the relationship between current through and voltage across the capacitor is Ic = C dv /dt Therefore

$$\frac{V_{in} - V_2}{R_1} = C_f \frac{d(V_2 - V_O)}{dt}$$

However, V_1=V_2 =0 (virtual ground Concept) because A is very large. Therefore, V_{in}/R_1 = C_f $\frac{d(-V_0)}{dt}$ The output voltage can be obtained by integrating both sides with respect to time. Therefore,

$$\text{Vo} = -\frac{1}{R_1 C_F} \int_0^t \boldsymbol{v_{in}}\, \boldsymbol{dt} + \text{C}$$

CIRCUIT DIAGRAM:-

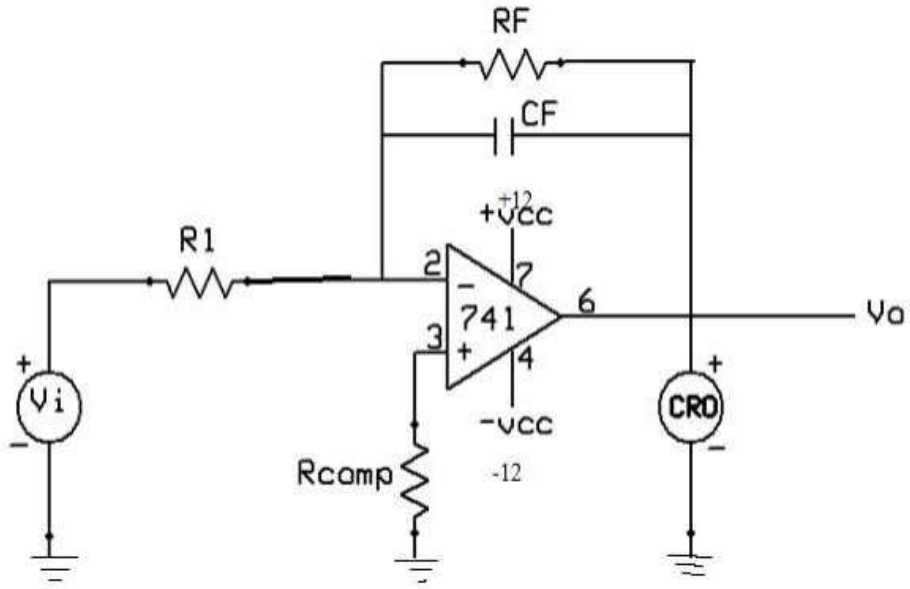

Fig. 13.1 Circuit Diagram of Integrator

DESIGN PROCEDURE:

To design an integrator circuit to integrate an input signal that varies in frequency from 10 Hz to about 1 KHz.

Let us: f_b= 1 KHz

We know the frequency at which the gain is 0 dB, $f_b = \frac{1}{2\pi R_1 C_F}$

Let us assume C_F = 0.1 µF; then

$$R_1 = \frac{1}{2\pi X\ 0.1\ X\ 10^{-6} X\ 1\ X\ 10^3}$$

R_1= 1592Ω OR 1600Ω

Since f_b = 10 f_a, f_a=0.1 KHz and also the gain limiting frequency , $f_a = \frac{1}{2\pi R_F C_F}$

$$R_F = \frac{1}{2\pi X\ 0.1\ X\ 10^{-6} X\ 0.1\ X\ 10^3}$$

R_F=15.923 KΩ OR 16KΩ

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATION:

Table 13.1 Output voltage with frequency

S.No	Input amplitude(V)	Frequency(Hz)	Output amplitude(V)	Frequency (Hz)

MODEL GRAPH:

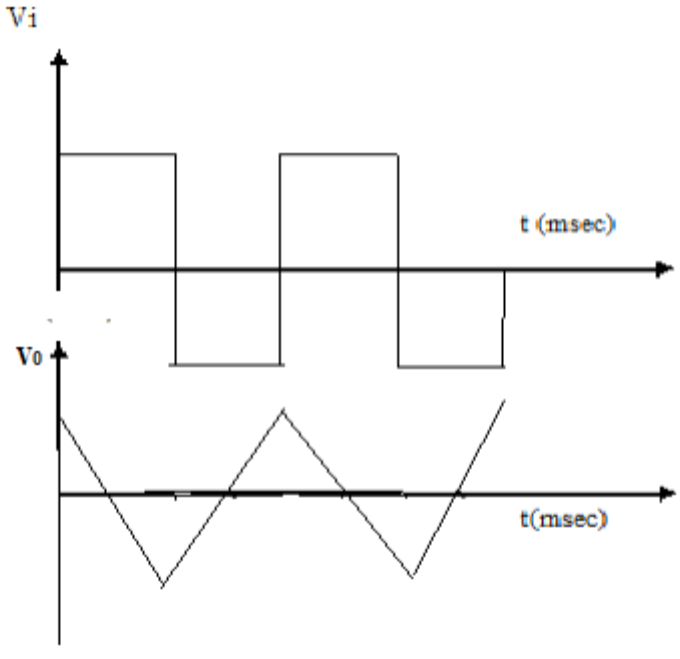

Fig .13.2 Input and output waveform of Integrator

RESULT:-

We have successfully designed a integrator circuit using Op-Amp to integrate an input signal that varies in frequency from 10 Hz to about 1 KHz.

Designed parameters are as follows:

R_1=1600 Ω, R_F=16KΩ

We have plotted input and output waveform for the designed integrator.

DISCUSSION:

1. What are the problems in an ordinary op-amp Integrator?
2. What are the changes in the circuit of a practical integrator?
3. What is a lossy integrator?
4. Why integrators are preferred over differentiators in electronic circuits?
5. What are the applications of integrators?

EXPERIMENT-14

AIM:-

Design a second order low pass filter for a particular cutoff frequency

APPARATUS REQUIRED:-

- Function generator
- CRO
- Multimeter
- Power Supply with Bread Board(+12V & -12V)

COMPONENT REQUIRED:-

OPAMP IC 741, desired values of resistors and capacitors

THEORY:

Second order Low Pass Filter

A first-order Butterworth low pass filter has the same magnitude and phase response characteristics as a passive RC filter with the exception of the fact that you can have gain in the pass band.

This circuit is a combination of two things: The first is a passive low pass filter (using capacitor C and resistor R). The second is a non – inverting op-amp combination using the op-amp and the three resistors.

A First order low pass filter can be converted into a second order type simple by using an additional RC network.

The gain of the second order filter is set by R_1 and R_F, while the high cutoff frequency F_H is determined by R_2, C_2,R_3 and C_3 as follows:

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$; High cutoff frequency of the filter

$$A_F = 1 + \frac{R_F}{R_1}$$;Passband gain of the input signal

The gain magnitude and phase angle equations of the LPF the can be obtained by converting V_0/V_{in} into its equivalent polar form as follows

$$\frac{V_0}{V_{in}} = \frac{A_F}{\sqrt{1+(\frac{f}{f_H})^4}}$$

Where:

$\frac{V_O}{V_i}$ =Gain of the filter as a function of frequency

f=Frequency of the input signal(Hz)

Steps for Filter Design:

The Design steps for second order filter are as follows:

I. Choose a value for the high cutoff frequency f_H.

II. To Simplify the design calculations, set R_2=R_3=R and C_2=C_3=C then choose a value of C≤1 μF.

III. Calculate the value of R using an equation

R=$\frac{1}{2\pi f_H C}$

IV. Finally, because of the equal resistor(R_2=R_3) and capacitor (C_2=C_3)values,the passband voltage gain A_F=1+$\frac{R_F}{R_1}$ of the second order low pass filter has to be equal to 1.586.That is R_F=0.586R1.This gain is necessary to guarantee a Butterworth response.Hence choose a value of R_1≤100KΩ and calculate the value of R_F

DESIGN PROCUDURE:

To design second order low pass filter,the steps are

i. f_H=1 kHz

ii. Let C_2=C_3=0.0047 μF

iii. Then,

R_2=R_3=$\frac{1}{2\pi(10^3)(47)(10^{-10})} = 33.86\ k\Omega$

(Use R_2=R_3=33kΩ)

iv. A_F(dB)=4=20 log(A_F)

A_F=1.586

Then

A_F=1+$\frac{R_F}{R_1}$

Since R_F must be equal to 0.586R_1, Let R_1 equal 27kΩ,Therefor,

R_F=(0.586)(27 kΩ)=15.82 kΩ

Thus the required component are

R_2=R_3=33 kΩ

C_2=C_3=0.0047 µF

R_1=27 kΩ and R_F=15.8 kΩ(20 kΩ pot)

CIRCUIT DIAGRAM:

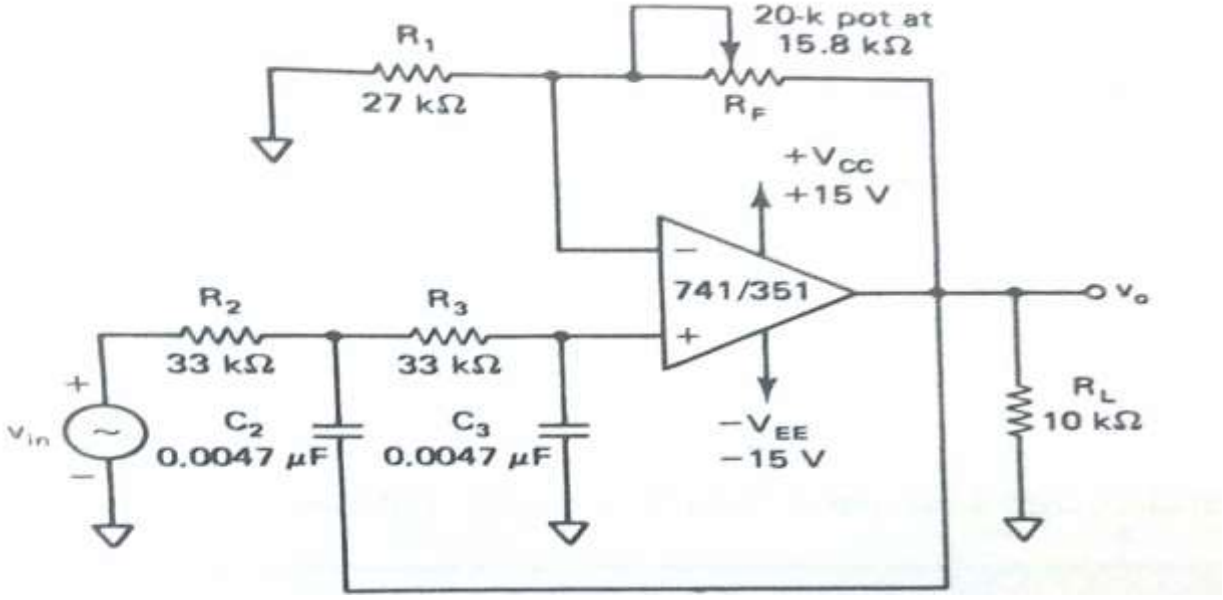

Fig.14.1 Ciruit Diagram of a second order low pass filter

PROCEDURE:-

Procedure for low pass filter

- To achieve the desired gain we have to calculate the value of R_2,R_3,R_F .
- Connect the circuit as shown in fig 14.1
- Apply AC input signal on pin 3 of IC 741.
- Observe the output on CRO.
- Repeat step 2 & 3 for different values of input signal.

- Trace the frequency response curve by changing the value of frequency of the input waveform.
- Obtain the 3db point of the frequency response curve.

OBSERVATION:-

Table 14.1 Observation for low pass filter

S.NO.	Frequency(Hz)	V_{in}	V_o	Gain Magnitude $A_v=\frac{v_0}{v_{in}}$	Magnitude(dB) $20\log \frac{v_0}{v_{in}}$
1	10				
2	100				
3	200				
4	700				
5	1000				
6	3000				
7	7000				
8	10000				
9	30000				
10	100000				

Frequency response of second order low pass filter:

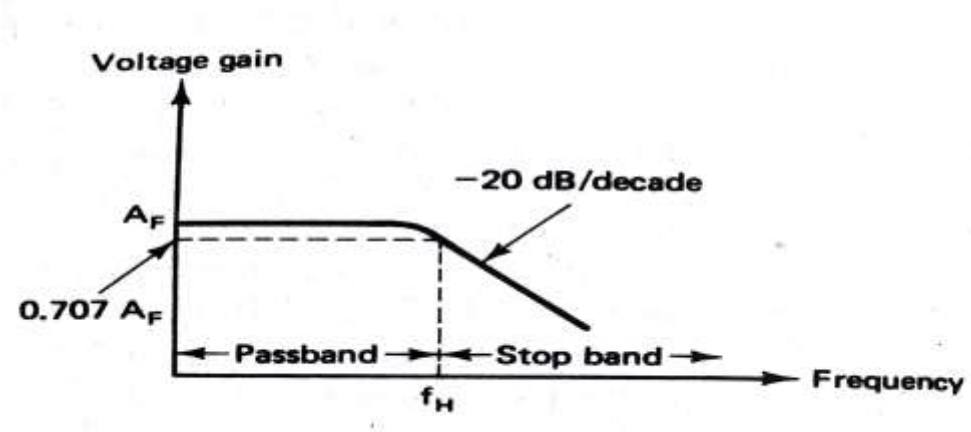

Fig.14.2 Frequency response of second order filter

RESULT:-

We have successfully designed a second order low pass filter of cut-off frequency 1 kHz with a pass band gain of 6 dB, using op-amp 741.

Designed parameters are as follows:

f_c= 1 kHz, A_f= 4dB, C_2=C_3=0.0047 µF, R_2=R_3=33 kΩ

R_1=27 kΩ and R_F=15.8 kΩ(20 kΩ pot)

We have plotted the frequency response curve for the designed filter. As per the frequency response curve, the output voltage is constant for low frequencies till 1 kHz and then decreases with frequency. Further, we observed that gain is also constant for lower frequencies up to 1 kHz and decreasing for higher frequencies.

DISCUSSION:

1. What are the advantages of active over passive ones?
2. What is the Butterworth response?
3. What is the difference between active and passive filters.
4. How is the frequency response are differ of first order and second order low pass filter.
5. What is the application of second order low pass filter.