



# **Techno India NJR Institute of Technology**

Department of Electronics & Communication Engineering

B.Tech. III Semester

Lab: Electronic Devices (3EC4-21)



# RAJASTHAN TECHNICAL UNIVERSITY, KOTA

## SYLLABUS

II Year - III Semester: B.Tech. (Electronics & Communication Engineering)

### 3EC4-21: Electronics Devices Lab

1 Credit

Max. Marks: 50 (IA:30, ETE:20)

0L:0T:2P

#### List of Experiments

Sr. No.	Name of Experiment
1.	Study the following devices: (a) Analog & digital multimeters (b) Function/Signal generators (c) Regulated d. c. power supplies (constant voltage and constant current operations) (d) Study of analog and digital CRO, measurement of time period, amplitude, frequency & phase angle using Lissajous figures.
2.	Plot V-I characteristic of P-N junction diode & calculate cut-in voltage, reverse Saturation current and static & dynamic resistances.
3.	Plot the output waveform of half wave rectifier and effect of filters on waveform. Also calculate its ripple factor.
4.	Study bridge rectifier and measure the effect of filter network on D.C. voltage output & ripple factor.
5.	Plot and verify output waveforms of different clipper and clamper.
6.	Plot V-I characteristic of Zener diode
7.	Study of Zener diode as voltage regulator. Observe the effect of load changes and determine load limits of the voltage regulator
8.	Plot input-output characteristics of BJT in CB, CC and CE configurations. Find their h-parameters.
9.	Study of different biasing circuits of BJT amplifier and calculate its Q-point.
10.	Plot frequency response of two stage RC coupled amplifier & calculate its bandwidth .
11.	Plot input-output characteristics of field effect transistor and measure $I_{dss}$ and $V_p$ .
12.	Plot frequency response curve for FET amplifier and calculate its gain bandwidth product.

Office of Dean Academic Affairs  
Rajasthan Technical University, Kota



# RAJASTHAN TECHNICAL UNIVERSITY, KOTA

## SYLLABUS

II Year - III Semester: B.Tech. (Electronics & Communication Engineering)

### Course Outcome:

Course Code	Course Name	Course Outcome	Details
3EC4-21	Electronic Devices Lab	CO 1	Understand the characteristics of different Electronic Devices.
		CO 2	Verify the rectifier circuits using diodes and implement them using hardware.
		CO 3	Design various amplifiers like CE, CC, common source amplifiers and implement them using hardware and also observe their frequency responses
		CO 4	Understand the construction, operation and characteristics of JFET and MOSFET, which can be used in the design of amplifiers.
		CO 5	Understand the need and requirements to obtain frequency response from a transistor so that Design of RF amplifiers and other high frequency amplifiers is feasible

### CO-PO Mapping:

Subject	Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
3EC4-21 Electronic Devices Lab	CO 1	3	2	3	2	1							1
	CO 2	2	3	1	3	3							2
	CO 3	2	1	2	3	3							
	CO 4	3	2	3	2	2							1
	CO 5	3	2	1	2	2							

**3: Strongly**

**2: Moderate**

**1: Weak**

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## EXPERIMENT NO:-1

**Object:-** Study the following devices:

- (a) Analog & digital multi meters
- (b) Function/ Signal generators
- (c) Regulated d. c. power supplies (constant voltage and constant current operations)
- (d) Study of analog CRO, measurement of time period, amplitude, frequency & phase angle using Lissajous figures.

**Equipments Required:-**

S No.	Equipment	Range	Quantity
1.	Power supply	(0 to 30) v	1
2.	CRO	30MHz	1
3.	Function Generator	3 MHz	1
4.	Multimeter		1
5.	connecting wires		

**Theory:**

### 1.1 Regulated Power Supply

Power supplies provided by a regulated DC voltage facilities fine and coarse adjustments and monitoring facilities for voltage and current. They will work in constant voltage and current mode depending on current limit and output load. The current limit has good stability, load and line regulations. Outputs are protected against overload and short circuit damages. They are available in single and dual channel models with different voltage and current capacities. Overload protection circuit of constant self restoring type is provided to prevent the unit as well as the circuit under use. The power supplies are specially designed and developed for well regulated DC output. These are useful for high regulation laboratory power supplies, particularly suitable for experimental setup and circuit development in R&D.

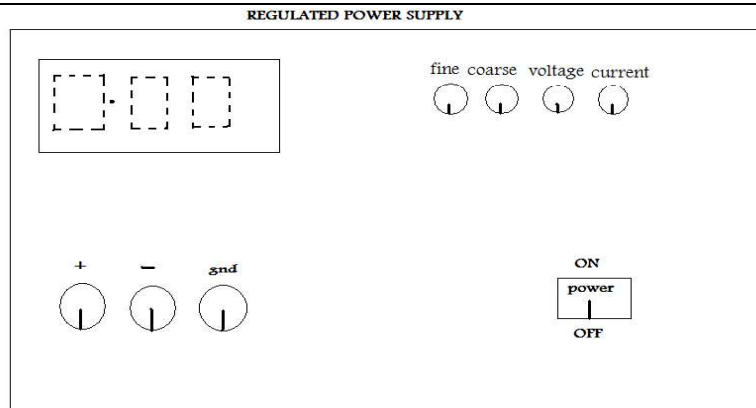


Fig.1.1 Front Panel of Power Supply

## 1.2 Function Generator

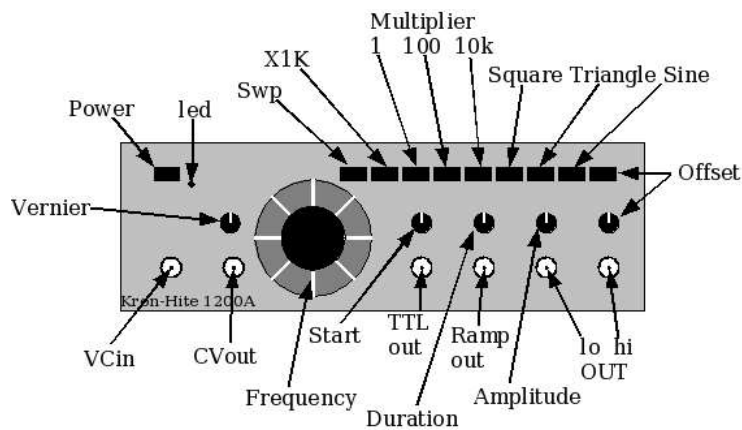


Fig.1.2 Front panel of Function Generator

Designation	Specifications
Wave form	: Sine, squares, triangles, TTL square waves
Amplitude	: 0-20V for all the functions.
Sine distortion	: Less than 1% from 0.1 HZ to 100 HZ harmonics Modulation showed down fundamental for 100K HZ to 1MHG.
Offset	: Continuously variable 10V
Frequency range	: 0.1 HZ to 1Mhz in ranges.
Output impedance	: 600 ohms, 5%.
Square wave duty cycle	: 49% to 51%.

**Range selectors:** Decode frequency by multiplying the range selected with the frequency indicated by dial gives the output frequency, which applies for all functions.

**Function selectors:** Selected desired output wave form which appears at 600Ω output.

**VCO input:** An external input will vary the output frequency. The change in frequency is directly proportional to input voltage.

**TTL output:** A TTL square wave is available at this jack. The frequency is determined by the range selected and the setting of frequency dial. This output is independent of amplitude and D.C OFFSET controls.

**Amplitude control:** Control the amplitude of the output signal, which appears at 600ohms.

**OFFSET control:** Control the DC offset of the output. It is continuously variable for  $\pm 5V$ ,  $\pm 100V$ .

**Fine frequency dial:** Multiplying the setting of this dial to the frequency range selected gives the output frequency of the wave forms at the 600ohms..

## 1.3 Multimeter:

### Digital Multimeter

A multimeter is a versatile instrument and is also called Volt-Ohm-Milliammeter (VOM). It is used to measure the d.c and a.c voltages and resistance values. A digital multimeter essentially consists of an analog to digital converters. It converts analog values in the input to an equivalent binary forms. These values are processed by digital circuits to be shown on the visual display with decimal values. The liquid crystal display system is generally employed. Actually all the functions in DMM depend on the voltage measurements by the converter and comparator circuits

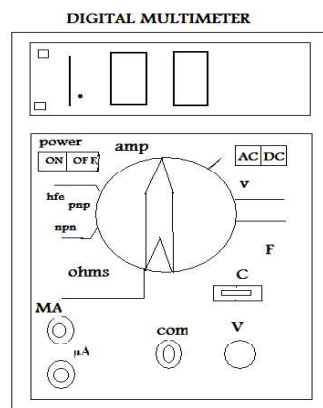


Fig.1.3 Digital Multimeter

**1.4 CRO:** C.R.O is a versatile instrument used for display of wave forms and is a fast x-y plotter. The heart of C.R.O is and the rest is the circuitry to operate C.R.O

The main parts are

1. Electron gun: - it is used to produce sharply focused beam of electron accelerated to very high velocity.
2. Deflection system: - it deflects the electron both in horizontal and vertical plan.
3. Florescent screen:- the screen which produces, spot of visible light . When beam of electrons are incident on it the other side of tube is coated with phosphorus material.

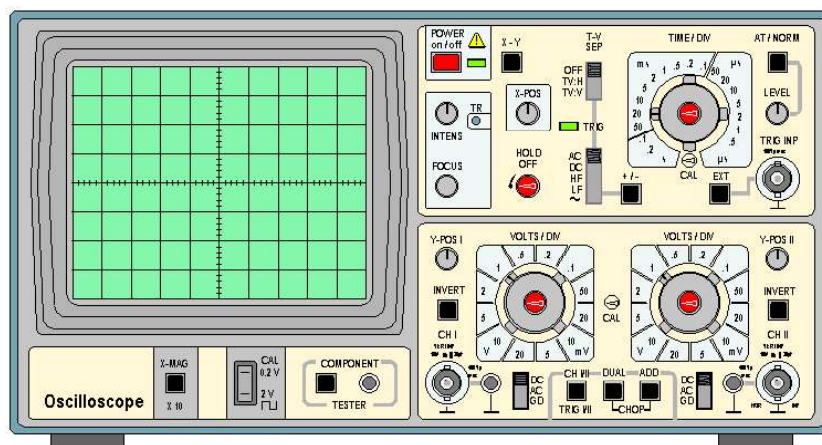


Fig.1.4 CRO

### Front Panel:

**ON-POWER:** toggle switch for switching on power.

**INTENCITY:** controls trace intensity from zero to maximum.

**FOCUS:** It controls sharpness of trace a slight adugestement of focus is done after changing intensity of trace.

**AC-DC: GROUND:** It selects coupling of AC-DC ground signal to vertical amplifier.

**X-MAG:** It expands length of time base from 1-5 times continuously and to maximum time base to 40 ns/cm.

**SQUARE:** This provides square wave 2v (p-P) amplitude and enables to check y calibration of scope.

**SAWTOOTH WAVE FORM:**

This provides saw tooth wave form output coincident to sweep speed with an output of saw tooth wave (p-p)

**VERTICAL SECTION:** y position:

This enables movement of display along y-axis.

**Y-INPUT:** It connects input signal to vertical amplifier through AC-DC ground coupling switch

**CALIBRATION:** 15mv – 150mv dc signal depending on position selection is applied to vertical amplifier.

**DC BALANCE:** It is control on panel electrostatic ally in accordance with waveforms to be displayed.

**VOLTS/CM:** Switch adjusts sensitivity.

**HORIZONTAL SECTION: X-POSITION:** This control enables movement of display along x-axis.

**TRIGGERING LEVEL:** It selects mode of triggering.**TIMEBASE:** This controls or selects sweep speeds.

**VERNUIS:** This control the fine adjustments associated with time base sweep.

**SIGN SELECTOR:** It selects different options of INT/EXT, NORM/TO.

**STAB:** Present on panel



**EXITCAD:** It allows time base range to be extended.

**HORIZONTAL INPUT:** It connects external signal to horizontal amplifier.

**Ext SYN:** it connects external signal to trigger circuit for synchronization.

### **OBSERVATIONS:-**

Amplitude = no. of vertical divisions \* Volts/div.

Time period = no. of horizontal divisions \* Time/div.

Frequency=1/T

Amplitude taken on vertical section (y).

Time period taken on horizontal section(x)

### **Model Wave Forms:**

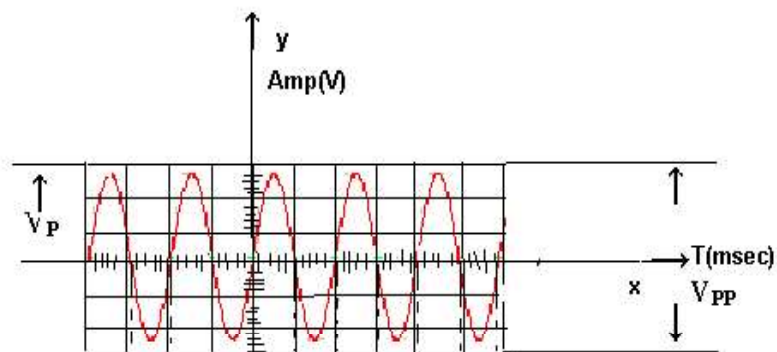


Fig.1.5 Wave form on CRO

### **Applications of CRO:**

1. Measurement of current
2. Measurement of voltage
3. Measurement of power
4. Measurement of frequency
5. Measurement of phase angle

6. To see transistor curves
7. To trace and measuring signals of RF, IF and AF in radio and TV.
8. To trace visual display of sine waves.

**Result:** To calculate the given waveform, frequency, amplitude and phase.

**Viva Question:-**

1. What is CRO?
2. Show the different component pattern on CRO?
3. Between which quantities CRO graph is represented?
4. How can you measure the AC and DC voltage and current on multimeter.
5. What is different part of CRT?
6. What is the method of focusing used in CRO?
7. How many types of sweeps used in CRO?
8. What are sources of synchronization?
9. What is function generator?
10. Difference between the digital and analog millimeter.
11. Explain the use of db in function generator.
12. What is the voltage range of function generator?
13. How we calculate the frequency in CRO?
14. How we calculate the Amplitude in CRO?
15. What is the frequency of DC wave?

## EXPERIMENT NO:-2

**Object:-** Plot V-I characteristic of P-N junction diode & calculate cut-in voltage, reverse

Saturation current and static & dynamic resistances.

**Equipment:-**

S No.	Equipment	Range	Quantity
	Power supply	(0 to 30) v	1
	P-N Diode IN4007.		1
	Resistor	1K $\Omega$	1
	Ammeters	(0-100 mA, 0-500 $\mu$ A)	1
	Voltmeter	(0-20 V,0-1V)	1
	connecting wires		

**Theory:-**

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to -ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage. When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected -ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

### Circuit Diagram:-

#### Forward Bias:-

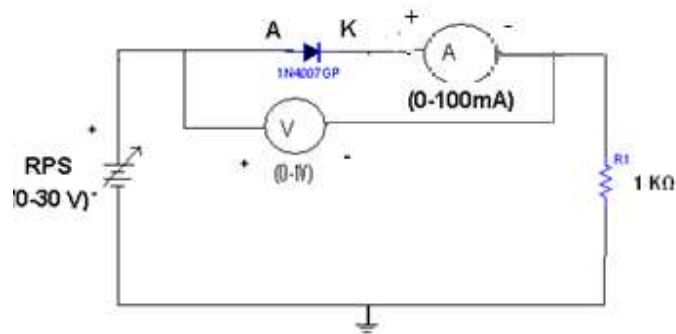


Fig.2.1 Forward Bias Characteristics

#### Reverse Bias:-

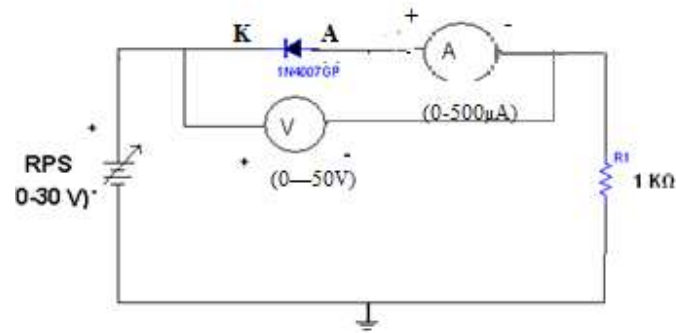


Fig.2.2 Reverse Bias Characteristics

#### Model Waveform:-

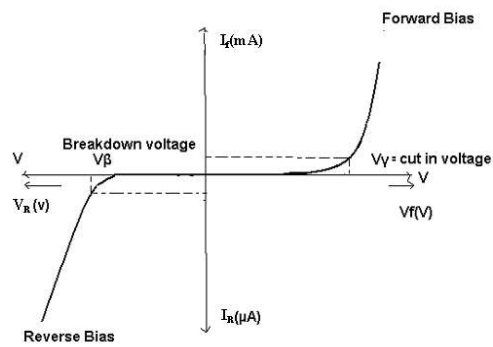


Fig.2.3 V-I characteristic of PN diode

**Procedure:-**

**Forward Bias:-**

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS -ve is connected to the cathode of the diode,
3. Switch on the power supply and increases the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage and current.

**Observation:-**

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

Table 2.1

**Procedure:-**

**Reverse Bias:-**

1. Connections are made as per the circuit diagram
2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS -ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in Steps
4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage and current.

**Observation:-**

S.NO	APPLIED VOLTAGE ACROSS DIODE(V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

Table 2.2

**Precautions:-**

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

**Result: -** Forward and Reverse Bias characteristics for a p-n diode is observed

**Viva Questions:-**

1. Define depletion region of a diode?
2. What is meant by transition & space charge capacitance of a diode?
3. Is the V-I relationship of a diode Linear or Exponential?
4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
5. What are the applications of a p-n diode?
6. Draw the ideal characteristics of P-N junction diode?
7. What is the diode equation?
8. What is PIV?
9. What is the break down voltage?
10. What is the effect of temperature on PN junction diodes?
11. What is the typical conduction voltage for a silicon diode?
12. What would be a typical magnitude for the reverse current in general purpose silicon diode?
13. What is diode current?

## EXPERIMENT NO:-3

**Object:** - Study half wave rectifier and effect of filters on wave. Also calculate theoretical & practical ripple factor.

1. with Filter
2. without Filter

### Apparatus Required:-

S.No.	Apparatus	Specification	Quantity
1.	Diode	1N 4007	1
2.	Transformer	(6-0-6).	1
2.	Capacitor	100 $\mu$ f	1
	Resistor	1K $\Omega$	1
3.	Connecting wires	-	

### Theory: -

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage. During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p

voltage is the value measured on dc voltmeter. For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

## Circuit Diagram:-

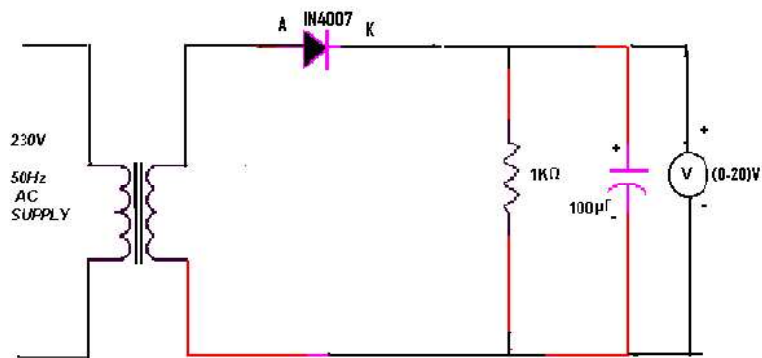


Fig.10.1 Circuit Diagram of Half Wave Rectifier

## Procedure:-

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Find the theoretical of dc voltage by using the formula,

$$V_{dc} = V_m / \pi$$

Where,  $V_m = 2V_{rms}$ , ( $V_{rms}$ =output ac voltage.)

The Ripple factor is calculated by using the formula

$r = \text{ac output voltage} / \text{dc output voltage}$ .

## Regulation Characteristics:-

1. Connections are made as per the circuit diagram.
2. By increasing the value of the rheostat, the voltage across the load and current flowing through the load are measured.
3. The reading is tabulated.
4. Draw a graph between load voltage ( $V_L$ ) and load current ( $I_L$ ) taking  $V_L$  on X-axis and  $I_L$  on y-axis
5. From the value of no-load voltages, the %regulation is calculated using the formula,



## Theoretical calculations for Ripple factor:-

### Without Filter:-

$$V_{rms} = V_m / 2$$

$$V_m = 2V_{rms}$$

$$V_{dc} = V_m / \pi$$

$$\text{Ripple factor } r = \sqrt{(V_{rms} / V_{dc})^2 - 1} = 1.21$$

### With Filter:-

$$\text{Ripple factor, } r = 1 / (2\sqrt{3} f C R)$$

$$\text{Where } f = 50\text{Hz}$$

$$C = 100\mu\text{F}$$

$$R_L = 1\text{K}\Omega$$

## Practical Calculations:-

$$V_{ac} =$$

$$V_{dc} =$$

$$\text{Ripple factor without Filter} =$$

$$\text{Ripple factor with Filter} =$$

## Observations:-

### Without Filter

USING DMM	$V_{ac}(v)$	$V_{dc}(v)$	$r = V_{ac} / V_{dc}$

Table.10.1

**With Filter**

<b>USING DMM</b>	<b>V<sub>ac</sub>(v)</b>	<b>V<sub>dc</sub>(v)</b>	<b>r= V<sub>ac</sub>/ V<sub>dc</sub></b>

Table.10.2

**Without filter:-**

$V_{dc}=V_m/\pi, \quad V_{rms}=V_m/2, \quad V_{ac}=\sqrt{(V_{rms}^2- V_{dc}^2)}$

<b>USING CRO</b>	<b>V<sub>m</sub>(v)</b>	<b>V<sub>ac</sub>(v)</b>	<b>V<sub>dc</sub>(v)</b>	<b>r= V<sub>ac</sub>/ V<sub>dc</sub></b>

Table.10.3

**With filter**

<b>USINGCRO</b>	<b>V<sub>1</sub>(V)</b>	<b>V<sub>2</sub>(V)</b>	<b>V<sub>dc</sub>= (V<sub>1</sub>+V<sub>2</sub>)/2</b>	<b>V<sub>ac</sub>= (V<sub>1</sub>- V<sub>2</sub>)/2√3</b>	<b>r= V<sub>ac</sub>/ V<sub>dc</sub></b>

Table.10.4

**Precautions:**

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

**Result:-**

1. The Ripple factor for the Half-Wave Rectifier with and without filters is measured.
2. The % regulation of the Half-Wave rectifier is calculated.

**Viva Questions:**

1. What is the efficiency of half wave rectifier?
2. What is the rectifier?
3. What is the difference between the half wave rectifier and full wave Rectifier?
4. What is the o/p frequency of Bridge Rectifier?
5. What are the ripples?
6. What is the function of the filters?
7. What is TUF?
8. What is the average value of o/p voltage for HWR?
9. What is the peak factor?
10. If the ac supply is 60 Hz, what will be the ripple frequency of output the half wave rectifier?
11. A silicon diode in a half wave rectifier has a barrier potential of 0.7 V. What is the effect of this?
12. What is the  $V_{RRM}$  for the IN4001 rectifier diode?
13. An open circuit can have any voltage across its terminals then what will the current?
14. By which value of the filter capacitor input ripple factor can be lowered?
15. What is the PIV of Half wave rectifier

## EXPERIMENT NO:-4

**Object:** - Study bridge rectifier and measure the effect of filter network on D.C. voltage output & ripple factor.

### Apparatus Required:-

S.No.	Apparatus	Specification	Quantity
1.	Diode	1N 4007	4
2.	Transformer	(6-0-6).	1
2.	Capacitor	100 $\mu$ f	1
	Resistor	1K $\Omega$	1
3.	Connecting wires	-	

### THEORY:-

The bridge rectifier is also a full-wave rectifier in which four p-n diodes are connected in the form of a bridge fashion. The Bridge rectifier has high efficiency when compared to half-wave rectifier. During every half cycle of the input, only two diodes will be conducting while other two diodes are in reverse bias.

### Circuit Diagram:-

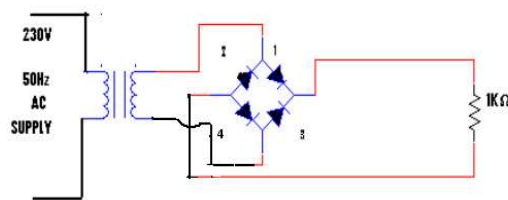


Fig.11.1 Circuit Diagram of Full Wave Rectifier

### **Procedure:-**

1. Connections are made as per the circuit diagram.
2. Connect the ac main to the primary side of the transformer and secondary side to the bridge rectifier.
3. Measure the ac voltage at the input of the rectifier using the multi meter.
4. Measure both the ac and dc voltages at the output of the Bridge rectifier.
5. Find the theoretical value of dc voltage by using the formula,

### **Calculations:-**

#### **Theoretical calculations:-**

$$V_{rms} = V_m / \sqrt{2}$$

$$V_m = V_{rms} \sqrt{2}$$

$$V_{dc} = 2V_m / \pi$$

#### **(i) Without filter:**

$$\text{Ripple factor, } r = \sqrt{(V_{rms} / V_{dc})^2 - 1} = 0.482$$

#### **(ii) With filter:**

$$\text{Ripple factor, } r = 1 / (4\sqrt{3} f C R_L) \quad \text{where } f = 50\text{Hz}$$
$$C = 100\mu\text{F}$$
$$R_L = 1\text{K}\Omega$$

### **Practical Calculations:-**

#### **Without filter:-**

$$V_{ac} =$$

$$V_{dc} =$$

$$\text{Ripple factor, } r = V_{ac} / V_{dc}$$

#### **With filters:-**

$$V_{ac} =$$

$$V_{dc} =$$

$$\text{Ripple factor, } r = V_{ac} / V_{dc}$$

**Observations:-**

**Without Filter**

USING DMM	V <sub>ac</sub> (v)	V <sub>dc</sub> (v)	r= V <sub>ac</sub> / V <sub>dc</sub>

Table.11.1

**With Filter**

USING DMM	V <sub>ac</sub> (v)	V <sub>dc</sub> (v)	r= V <sub>ac</sub> / V <sub>dc</sub>

Fig.11.2

**Without Filter:-**

$V_{rms} = V_m / \sqrt{2}$  ,  $V_{dc} = 2V_m / \Pi$  ,  $V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$

	V <sub>m</sub> (v)	V <sub>ac</sub> (v)	V <sub>dc</sub> (v)	r= V <sub>ac</sub> / V <sub>dc</sub>
USING CRO				

Table.11.3

**With Filter:-**

USINGCRO	V <sub>1</sub> (V)	V <sub>2</sub> (V)	V <sub>dc</sub> = (V <sub>1</sub> +V <sub>2</sub> )/2	V <sub>ac</sub> = (V <sub>1</sub> -V <sub>2</sub> )/2√3	r= V <sub>ac</sub> / V <sub>dc</sub>
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Table.11.4

**Waveform:-**

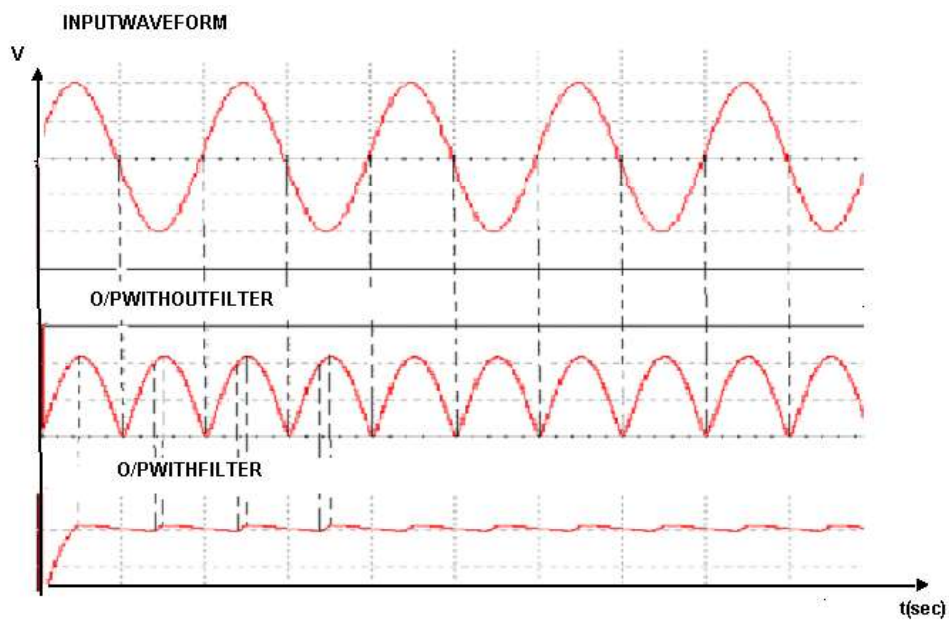


Fig.11.2

**Precautions:-**

1. The voltage applied should not exceed in the ratings of the diode
2. The diodes will be connected correctly

**Result:-**

The Ripple factor of Bridge rectifier is with and without filter calculated.

**Viva questions:-**

1. What is the PIV of Bridge rectifier?
2. What is the efficiency of Bridge rectifier?
3. What are the advantages of Bridge rectifier?
4. What is the difference between the Bridge rectifier and full wave rectifier?
5. What is the o/p frequency of Bridge Rectifier?
6. What is the disadvantage of Bridge Rectifier?
7. What is the maximum secondary voltage of a transformer?
8. What are the different types of the filters?
9. What is the difference between the Bridge rectifier and half wave Rectifier?
10. What is the maximum DC power delivered to the load?
11. Define regulation of the full wave?
12. Define peak inverse voltage? And write its value for full wave rectifier?
13. Explain how capacitor helps to improve the ripple factor?
14. What is the PIV for each diode in a full wave center-tapped rectifier?
15. What is application of rectifier?



## EXPERIMENT NO:-5

**Object:** - Plot and verify output waveform of different clipper & clamper

**Components Required:**

S.No.	Component	Value	Quantity
1.	Regulated power supply	(0-30V)	1
2.	Diode	1N3020(10v)	1
4.	Resistor	100K $\Omega$ 1K $\Omega$	1 1
5.	Signal generator	1MHz	1
6.	Connecting wire	-	-
7.	CRO	20MHz	1
8.	Capacitor	1 $\mu$ F	1

**Theory:-**

Clippers clip off a portion of the input signal without distorting the remaining part of the waveform. In the positive clipper shown above the input waveform above  $V_{ref}$  is clipped off. If  $V_{ref} = 0V$ , the entire positive half of the input waveform is clipped off.

Plot of input  $V_i$  (along X-axis) versus output  $V_o$  (along Y-axis) called transfer

Characteristics of the circuit can also be used to study the working of the clippers.

For stiff clipper:  $100R_B < R_S < 0.01R_L$ , Where  $R_B$  is bulk resistance of the diode. For diode IN914, value of  $R_B$  is  $30\Omega$ . Series resistor  $R_S$  must be 100times greater than bulk resistance  $R_B$  and 100 times smaller than load resistance  $R_L$ . If  $R_B = 30\Omega$  select  $R_S = 1k\Omega$  and  $R_L = 100k\Omega$ .

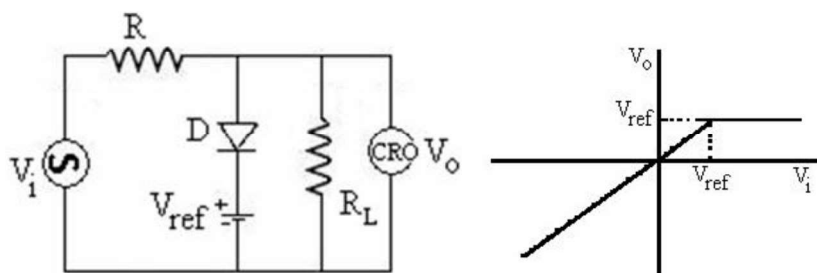


Fig.6.1 circuit diagram of positive clipper

### Procedure:

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator ( $V_i$ ) apply a sine wave of 1KHz frequency and a peak-to peak amplitude of 10V to the circuit. (Square wave can also be applied.)
4. Keep the CRO in dual mode; connect the input ( $V_i$ ) signal to channel 1 and output waveform ( $V_o$ ) to channel 2. Observe the clipped output waveform which is as shown in fig. Also record the amplitude and time data from the waveforms.
5. Now keep the CRO in X-Y mode and observe the transfer characteristic waveform.

### Waveforms

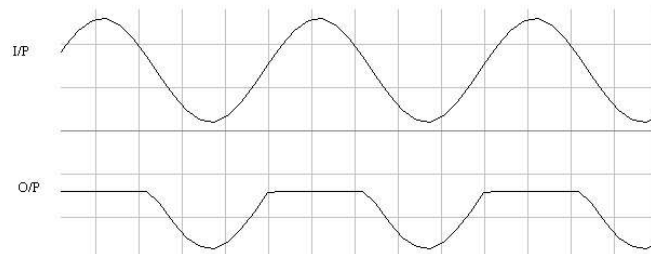


Fig.6.2 Input and output waveform for positive Clipper

### Double Ended Clipper:-

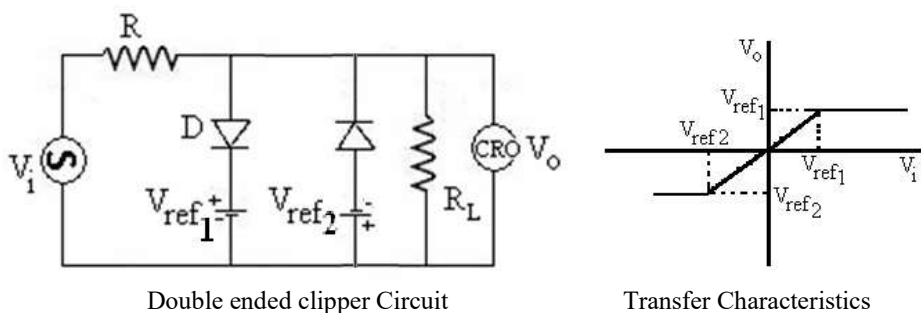


Fig.6.3

Apply  $V_i = 10 V_{pp}$  at 1kHz  
 $V_1 = 2V$   
 $V_2 = -2V$

## Wave Forms

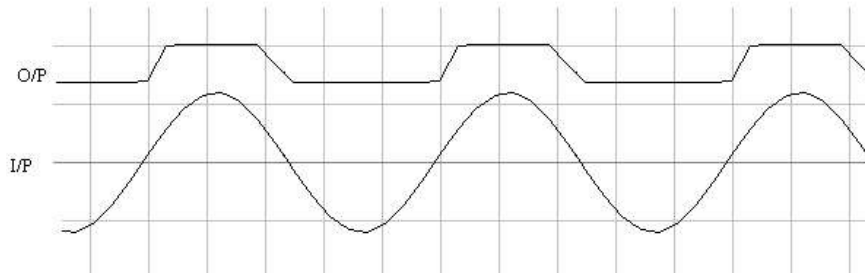


Fig.6.4 Input and output waveform for double-ended clipping circuit

The clamping network is one that will “clamp” a signal to a different DC level. The network must have a capacitor, a diode and a resistive element, but it can also employ an independent DC supply ( $V_{ref}$ ) to introduce an additional shift. The magnitude of R and C must be chosen such that time constant  $\tau = RLC$  is large enough to ensure the voltage across capacitor does not discharge significantly during the interval of the diode is non-conducting.

### Design:

For proper clamping,  $\tau > 100T$  where T is the time period of input waveform

If frequency is 1 kHz with peak-peak input voltage of 10V,  $T=1\text{ms}$

$$\tau = RL.C = 100 \times T = 100\text{ms}$$

Let  $C=1\mu\text{F}$

$$RL = 100 \times 10^{-3} = 100\text{k}\Omega$$

$$1 \times 10^{-6}$$

Select  $C = 1\mu\text{F}$  and  $RL = 100\text{ k}\Omega$

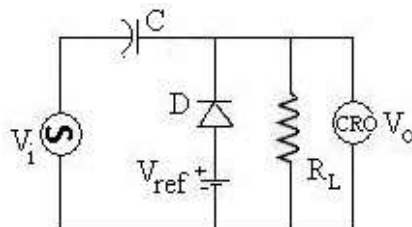


Fig.6.5 Positive Clamper

## Procedure:

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram
3. Using a signal generator apply a square wave input ( $V_i$ ) of peak-to-peak amplitude of 10V (and frequency greater than 50Hz) to the circuit.
4. Observe the clamped output waveform on CRO which is as shown in Fig.

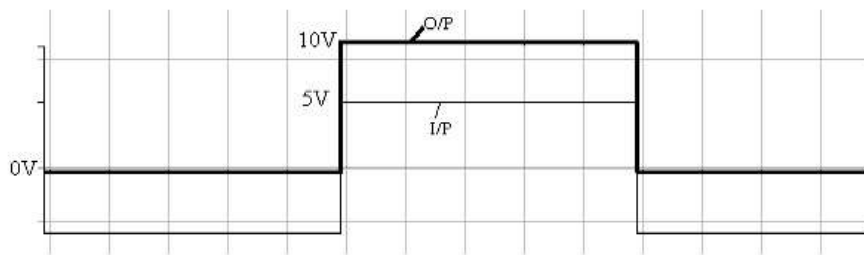


Fig.6.6 Input and output waveform for positive clamper without reference voltage

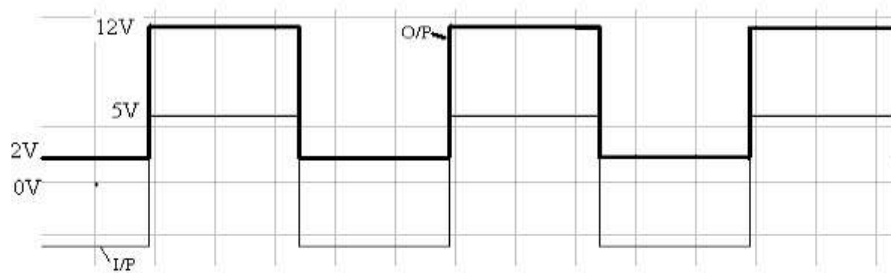


Fig.6.7 Input and output waveform for positive clamper circuit with reference voltage = 2V

## Result:

Output voltage  $V_0 =$  \_\_\_\_\_ during positive half cycle  
 $=$  \_\_\_\_\_ during negative half cycle

With  $V_{ref} = 0$ , output voltage  $V_0 =$  \_\_\_\_\_

With  $V_{ref} = 2$ , output voltage  $V_0 =$  \_\_\_\_\_

## Viva Questions:-

1. What is clamper?
2. What does positive clamper do and how?
3. What does negative clamper?
4. Why clamper circuit is also known as DC restorer circuit?
  
5. What is the position of diode in positive and negative half cycle of positive clamper?
6. What is biased clamper?
7. What is the output voltage of the positive and negative half cycle of positive clamper?
8. What is the output voltage of the positive and negative half cycle of negative clamper?
9. What are the applications of clamper circuits?
10. What is Clipper?
11. What is biased clipper?
12. What does positive clipper do and how?
13. What does negative clipper?
14. What type of diode circuit is used to clip off portions of signal voltage above or below certain levels?
15. What type of diode circuit is used to add or restore a dc level to an electrical signal?

## EXPERIMENT NO:-6

**Object:** - Plot V-I characteristic of zener diode.

**Apparatus:** -

S No.	Equipment	Range	Quantity
	Power supply	(0 to 30) v	1
	Zener diode.		1
	Resistor	1K $\Omega$	1
	Ammeters	(0-100 mA, 0-500 $\mu$ A)	1
	Voltmeter	(0-20 V,0-1V)	1
	connecting wires		

**Circuit Diagram:-**

**Static Characteristics:-**

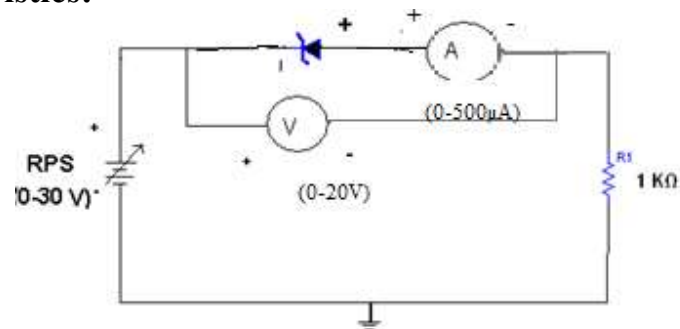


Fig.3.1 Reverse Bias Characteristics

**Regulation Characteristics:-**

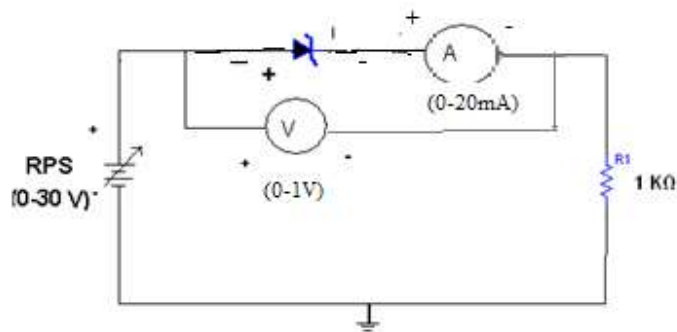


Fig.3.2 Forward Bias Characteristics

### **Theory:-**

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

### **Procedure:-**

#### **Static characteristics:-**

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The zener current ( $I_z$ ), and the zener voltage ( $V_z$ ) are observed and then noted in the tabular form.
4. A graph is plotted between zener current ( $I_z$ ) and zener voltage ( $V_z$ ).

#### **Regulation characteristics:-**

1. The voltage regulation of any device is usually expressed as percentage regulation
2. The percentage regulation is given by the formula
$$\frac{(V_{NL}-V_{FL})}{V_{FL}} \times 100$$
$$V_{NL} = \text{Voltage across the diode, when no load is connected.}$$
$$V_{FL} = \text{Voltage across the diode, when load is connected.}$$
3. Connection are made as per the circuit diagram
4. The load is placed in full load condition and the zener voltage ( $V_z$ ), Zener current ( $I_z$ ), load current ( $I_L$ ) are measured.
5. The above step is repeated by decreasing the value of the load in steps.
6. All the readings are tabulated.
7. The percentage regulation is calculated using the above formula

**Observations:-**

**Static characteristics:-**

S.NO	ZENER VOLTAGE( $V_Z$ )	ZENER CURRENT( $I_Z$ )

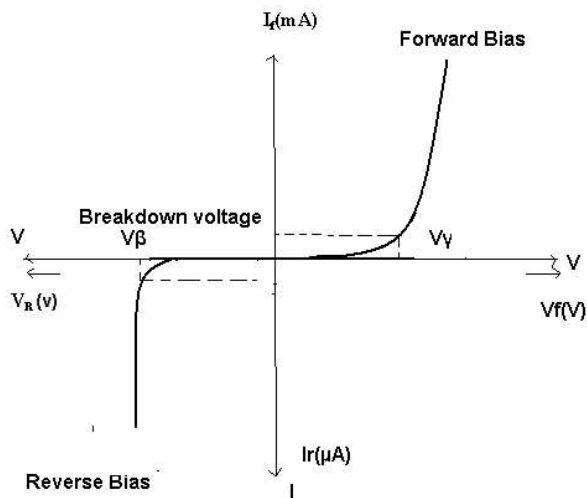
Table 3.1

**Regulation characteristics:-**

S.NO	$V_{NL}$ (VOLTS)	$V_{FL}$ (VOLTS)	$R_L$ ( $K\Omega$ )	% REGULATION

Table 3.2

**V-I characteristic of zener diode**





**Precautions:-**

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

**Result:-**

- a) Static characteristics of zener diode are obtained and drawn.
- b) Percentage regulation of zener diode is calculated.

**Viva questions:-**

1. What type of temp? Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impedance of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What are the difference between Avalanche and Zener breakdown?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?
11. Draw the V-I characteristic of zener diode?
12. Draw the symbol of zener diode?
13. Difference between zener diode and PN diode?
14. Doping level of zener diode is high or low?
15. The zener effect is valid approximately voltage level?

## EXPERIMENT NO:-7

**Object:** Study of Zener diode as a voltage regulator. Observe the effect of load changes and determine load limits of the voltage regulator.

### Equipment Required:

S No.	Equipment	Range	Quantity
1.	Power supply	(0 to 30) v	1
2.	Voltmeter	(0 to 20) v	1

### Component Required:

S.No.	Component	Value	Quantity
1.	Transistor	BC107	1
		2N3053A	1
2.	Zener diode	1N3020(10v)	1
4.	Resistor	330Ω	1
		100Ω	1
		470Ω	1
		4.7KΩ	1
		5.6KΩ	1
		1.5kΩ	1
		100KΩ	1
		1KΩ	1
5.	Potentiometer	5KΩ	1
		10KΩ	1
6.	Connecting wire	-	-

### Theory:

Regulator is a circuit, which maintains the terminal voltage constant even if input voltage varies or load current is varying.

**2.1 Shunt regulator:** The simplest form of voltage regulator uses a zener diode. This circuit gives more or less constant voltage irrespective of change in input voltage and load current. The unregulated voltage  $V_i$  is applied to the series current limiting resistor  $R_s$  and the regulated

output is taken across zener diode. A zener diode is in parallel with load, it is known as shunt regulator.

**2.2 Series regulator:** A low power zener diode is employed in simple regulator circuit, then the load current is limited by the maximum load current. In series voltage regulator, output is continuously sampled and then compared with a reference voltage any variation in the output is amplified and then fed to base of pass transistor. Negative feedback is used in this circuit.

**2.3 Load regulating** is the change in output voltage for a given change in load current (for example: "typically 15mV, maximum 100mV for load currents between 5mA and 1.4A, at some specified temperature and input voltage").

**2.4 line regulation** or input regulation is the degree to which output voltage changes with input (supply) voltage changes - as a ratio of output to input change (for example "typically 13mV/V"), or the output voltage change over the entire specified input voltage range (for example "plus or minus 2% for input voltages between 90V and 260V, 50-60Hz").

**Circuit diagram:**

**Shunt regulator:**

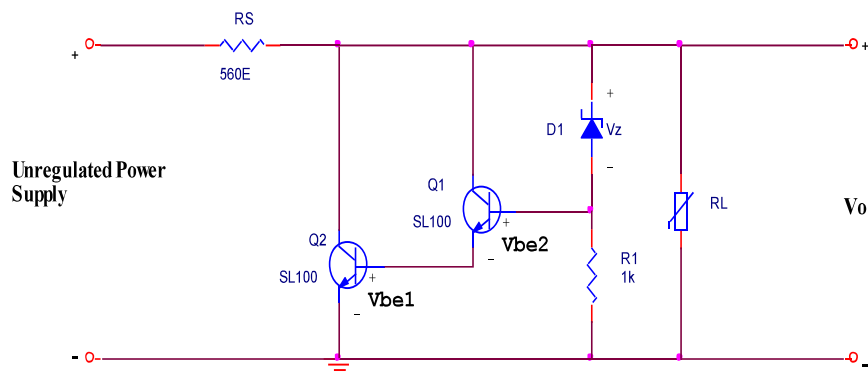


Fig 2.1 circuit diagram of Shunt voltage regulator

## Series regulator:

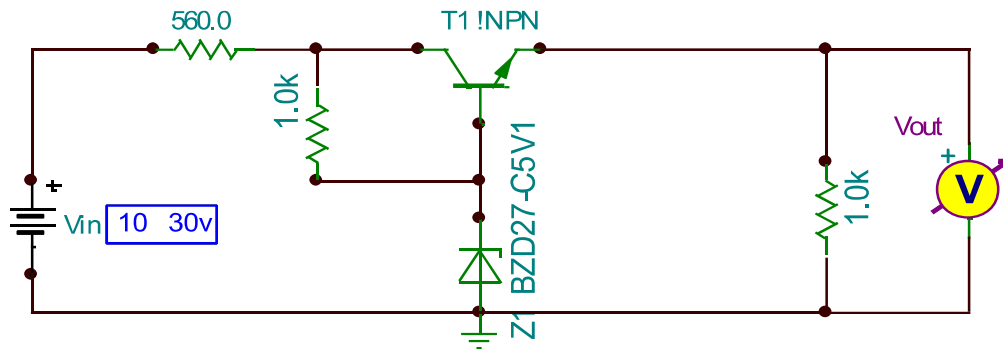


Fig 2.2 circuit diagram of Series voltage regulator

## Procedure:

### Line regulation-

- 1) Connect the circuit as per the circuit diagram.
- 2) Connect the load resistance of higher wattage (say  $1\text{K}\Omega$  /1W).
- 3) Vary the input DC supply in a regular step.
- 4) Note down the corresponding output voltage using a voltmeter.
- 5) Plot the graph:  $V_{in}$  vs.  $V_o$ .

### Load regulation-

- 1) For the same circuit shown, fix the input dc supply voltage, more than the regulating value.
- 2) Replace the fixed resistance by resistors of  $1\text{K}\Omega$ ,  $5\text{K}\Omega$ ,  $10\text{K}\Omega$  one by one.
- 3) Vary the load in regular steps.
- 4) Note down the corresponding output voltage across each load using voltmeter.
- 5) Plot the graph:  $V_o$  vs.  $R_L$ .

**Observation:**

**Shunt Regulator (line regulation)**

S No.	Input voltage ( $V_i$ ) (v)	Output voltage $V_o$ (v)

Table 2.1

**Shunt Regulator (load regulation) :**

S No.	Load resistance $R_L$ ( $\Omega$ )	Output voltage ( $V_o$ ) (v)

Table 2.2

**Series Regulation (line regulation) :**

S No.	Input voltage ( $V_i$ ) (v)	Output voltage $V_o$ (v)

Table 2.3

**Series Regulation (load regulation):**

S No.	Load resistance $R_L$ ( $\Omega$ )	Output voltage ( $V_o$ ) (v)

Table 2.4

### **Precautions:**

- 1) Connections on the breadboard should be tight.
- 2) Components should not touch each other.
- 3) Note down the reading carefully.
- 4) Connections should be neat and tight.

### **Result:**

Series and shunt regulators have been successfully constructed.

- 1) Shunt regulator- Line regulation= \_\_\_\_\_  
Load regulation= \_\_\_\_\_
- 2) Series regulator – Line regulation= \_\_\_\_\_  
Load regulation= \_\_\_\_\_

### **Discussion:**

A power amplifier supply having good voltage regulation shows the ability of that power supply to provide constant output voltage irrespective of change of input voltage, change in load current and temperature.

### **Viva Quiz:**

1. Define voltage regulator.
2. Give the advantages of series voltage regulator. .
3. Explain the feedback mechanism in series voltage regulator.
4. In series voltage regulator which is control element and explain its function.
5. Define load and line regulation. What is ideal value?
6. Which element determines output ripple?
7. What determines maximum load current allowed in this circuit?
8. Mention the applications of series voltage regulator.
9. Define no load voltage and full load voltage.
10. Explain the term percentage regulation.

11. Difference between zener diode and voltage regulation?
12. When used as voltage regulators, zener diodes are operated?
13. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?
14. Differentiate between line regulation & load regulation?
15. In which region zener diode can be used as a regulator?

## EXPERIMENT NO:-8

**Object:-**Plot input and output characteristics of BJT in CB, CC and CE configurations. Find their h parameters.

**Exp. No:-9(a):-**To observe and draw the input and output characteristics of a transistor connected in common base configuration.

### Apparatus Required:

S.No.	Component	Value	Quantity
1.	Transistor	BC107	1
2.	Voltmeter	(0-20V)	2
4.	Resistor	100Ω	1
5.	Regulated power supply	(0-30V)	1 1
6.	Ammeters	(0-100mA)	2
7.	Connecting wires		

### Theory:

A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration,  $I_E$  is +ve,  $I_C$  is -ve and  $I_B$  is -ve. So,

$$V_{EB}=f_1(V_{CB},I_E) \text{ and}$$

$$I_C=f_2(V_{CB},I_B)$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient within the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,  
 $\alpha = \Delta I_C / \Delta I_E$



## Circuit Diagram:

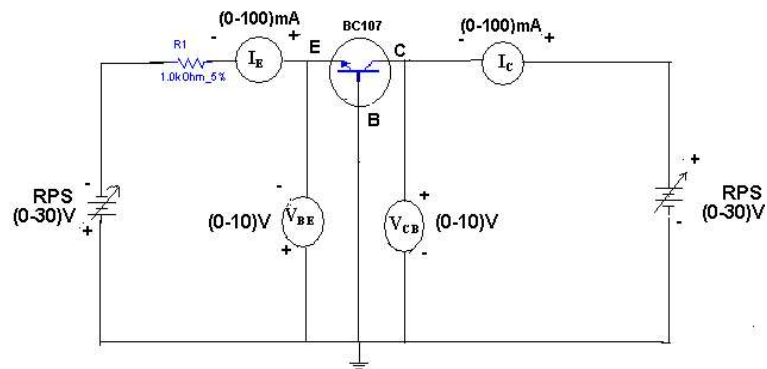


Fig.9 (a).1 Circuit Diagram of characteristics of BJT in CB

## Procedure:

### Input Characteristics:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage  $V_{CE}$  is kept constant at 0V and for different values of  $V_{EB}$  note down the values of  $I_E$ .
3. Repeat the above step keeping  $V_{CB}$  at 2V, 4V, and 6V. All the readings are tabulated.
4. A graph is drawn between  $V_{EB}$  and  $I_E$  for constant  $V_{CB}$ .

### Output Characteristics:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input  $I_E$  is kept constant at 10m A and for different values of  $V_{CB}$ , note down the values of  $I_C$ .
3. Repeat the above step for the values of  $I_E$  at 20 mA, 40 mA, and 60 mA, all the readings are tabulated.
4. A graph is drawn between  $V_{CB}$  and  $I_C$  for constant  $I_E$ .

**Observations:**

**Input Characteristics:**

S.No	$V_{CB}=0V$		$V_{CB}=1V$		$V_{CB}=2V$	
	$V_{EB}(V)$	$I_E(mA)$	$V_{EB}(V)$	$I_E(mA)$	$V_{EB}(V)$	$I_E(mA)$

Table9 (a).1

**Output Characteristics:**

S.No	$I_E=10mA$		$I_E=20mA$		$I_E=30mA$	
	$V_{CB}(V)$	$I_C(mA)$	$V_{CB}(V)$	$I_C(mA)$	$V_{CB}(V)$	$I_C(mA)$

Table9 (a).1.2

**Graphs :**

**Input Characteristics**

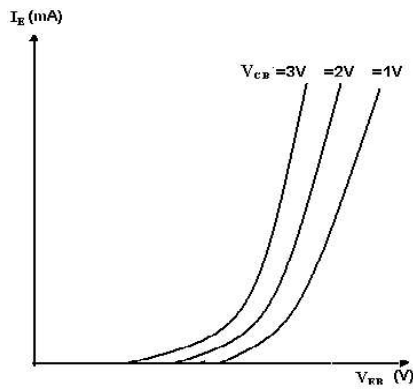


Fig.9 (a).2 Input Characteristics of CB Amplifier

## Output Characteristics:

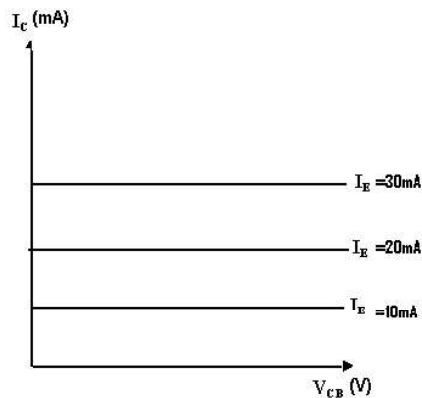


Fig.9 (a).3 Output Characteristics of CB

## Precautions:

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

## Result:

1. The input and output characteristics of the transistor are drawn.
2. The  $\alpha$  of the given transistor is calculated.

## VIVA QUESTIONS:

1. What is the range of  $\alpha$  for the transistor?
2. Draw the input and output characteristics of the transistor in CB configuration?
3. Identify various regions in output characteristics?
4. What is the relation between  $\alpha$  and  $\beta$ ?
5. What are the applications of CB configuration?
6. What are the input and output impedances of CB configuration?
7. Define  $\alpha$ (alpha)?
8. What is EARLY effect?
9. Draw diagram of CB configuration for PNP transistor

## EXPERIMENT No:-9

To draw the input and output characteristics of transistor connected in CE configuration

### Apparatus Required:

S.No.	Component	Value	Quantity
1.	Transistor	BC107	1
2.	Voltmeter	(0-20V)	2
4.	Resistor	1K $\Omega$	1
5.	Dual power supply	(0-30V)	1 1
6.	Ammeters	(0-100mA,0-500 $\mu$ A)	1,1
7.	Connecting wires		

### Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement  $I_B$  increases less rapidly with  $V_{BE}$ . Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between  $I_c$  and  $V_{CE}$  at constant  $I_B$ . the collector current varies with  $V_{CE}$  upto few volts only. After this the collector current becomes almost constant, and independent of  $V_{CE}$ . The value of  $V_{CE}$  up to which the collector current changes with  $V_{CE}$  is known as Knee voltage. The transistor always operated in the region above Knee voltage,  $I_c$  is always constant and is approximately equal to  $I_B$ . The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

## Circuit Diagram:

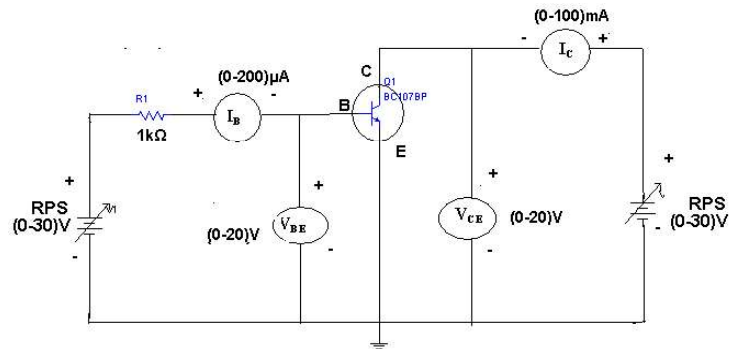


Fig.9(B).1 Circuit Diagram Of BJT Characteristics

## Procedure:

### Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage  $V_{CE}$  is kept constant at 1V and for different values of  $V_{BE}$ . Note down the values of  $I_C$
3. Repeat the above step by keeping  $V_{CE}$  at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between  $V_{BE}$  and  $I_B$  for constant  $V_{CE}$

### Output Characteristics:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current  $I_B$  is kept constant at 10μA and for different values of  $V_{CE}$  note down the values of  $I_C$
3. repeat the above step by keeping  $I_B$  at 75 μA 100 μA
4. tabulate the all the readings
5. plot the graph between  $V_{CE}$  and  $I_C$  for constant  $I_B$

**Observations:**

**Input Characteristics:**

S.NO	$V_{CE} = 1V$		$V_{CE} = 2V$		$V_{CE} = 4V$	
	$V_{BE}(V)$	$I_B(\mu A)$	$V_{BE}(V)$	$I_B(\mu A)$	$V_{BE}(V)$	$I_B(\mu A)$

Table.9 (b).1

**Out Put Characteristics:**

S.NO	$I_B = 50 \mu A$		$I_B = 75 \mu A$		$I_B = 100 \mu A$	
	$V_{CE}(V)$	$I_C(mA)$	$V_{CE}(V)$	$I_C(mA)$	$V_{CE}(V)$	$I_C(mA)$

Table 9(b).2

**Model Graphs:**

**Input Characteristics:**

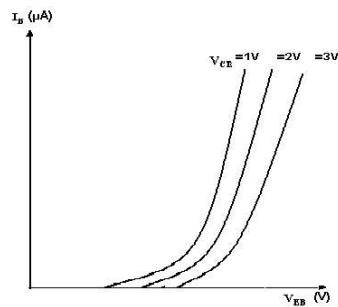


Fig.9 (B).2 Input Characteristics of BJT

## Output Characteristics:

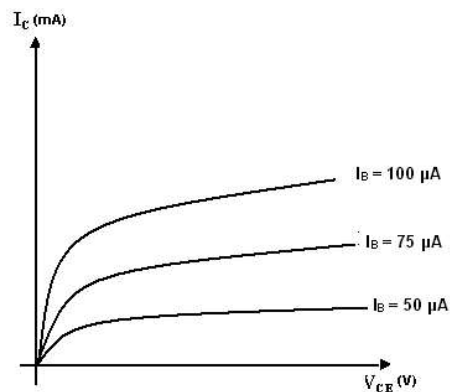


Fig.9(B).3 Output Characteristics of BIT

## Precautions:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

## Result:

1. the input and output characteristics of a transistor in CE configuration are Drawn
2. the  $\beta$  of a given transistor is calculated

## Viva Questions:

1. What is the range of  $\beta$  for the transistor?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. what is the relation between  $\alpha$  and  $\beta$
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration?
10. What are the applications of CE configuration?

## EXPERIMENT NO:-10

**Object:** - Plot gain- frequency response of two stages RC coupled amplifier & calculate its bandwidth.

### Apparatus:

S.No.	Component	Value	Quantity
1.	Transistor	BC107	2
2.	CRO	20MHz	1
4.	Resistor	1.5K	2
		33k	2
		15KΩ	2
		5.6k	2
5.	Regulated power supply	(0-30V)	1 1
6.	Capacitors	47uF, 10uF	2,3
7.	Function Generator	3MHz	1

### Theory:

This is most popular type of coupling as it provides excellent audio fidelity.

A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R1, R2, Re form biasing and stabilization network. Emitter bypass capacitor offers low reactance paths to signal coupling Capacitor transmits ac signal, blocks DC. Cascade stages amplify signal and overall gain is increased total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to  $A=A_1*A_2$

$A_1$ =voltage gain of first stage

$A_2$ =voltage gain of second stage.

When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor R<sub>c</sub>. It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in db. The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor C<sub>c</sub> and at high frequencies due to junction capacitance C<sub>be</sub>.



## Circuit Diagram:

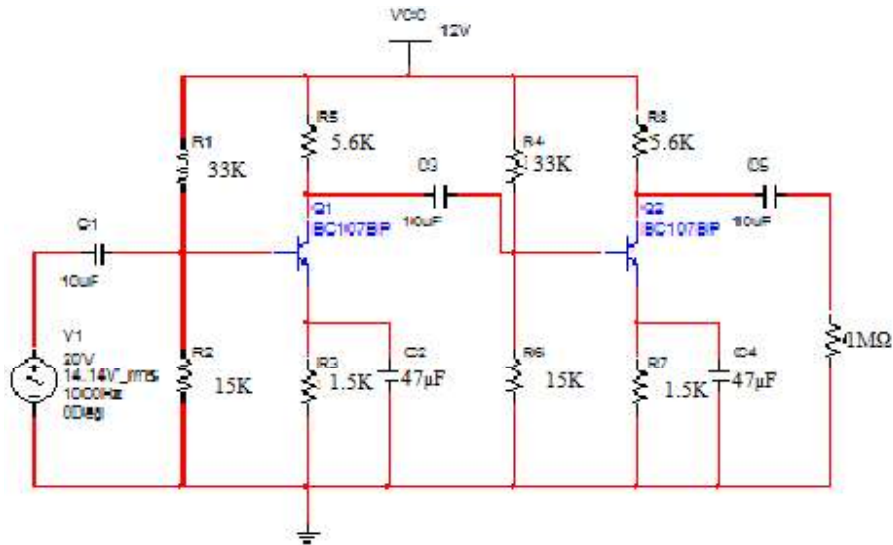


Fig.7.1 Circuit Diagram Of RC Coupled Amplifier

## Procedure:

1. Apply input by using function generator to the circuit.
2. Observe the output waveform on CRO.
3. Measure the voltage at
  - a. Output of first stage
  - b. Output of second stage.
4. From the readings calculate voltage gain of first stage, second stage and overall gain of two stages. Disconnect second stage and then measure output voltage of first stage calculates voltage gain.
5. Compare it with voltage gain obtained when second stage was connected.
6. Note down various values of gain for different frequencies.
7. A graph is plotted between frequency and voltage gain.

**Observations: -**

<b>FREQUENCY(Hz)</b>	<b>INPUT VOLTAGE (V<sub>i</sub>)</b>	<b>OUTPUT VOLTAGE (V<sub>o</sub>)</b>	<b>GAIN <math>A_v=(V_o/V_i)</math></b>	<b>GAIN IN dB <math>A_v=20\log_{10} (V_o/V_i)</math></b>

Table.7.1

**Model graph:-**

**Input Wave Form:**

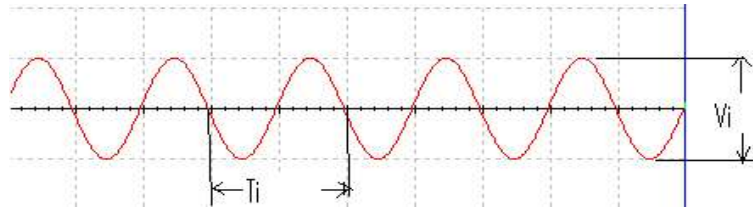


Fig.7.2 Input Wave Form for circuit

**First Stage Output:**

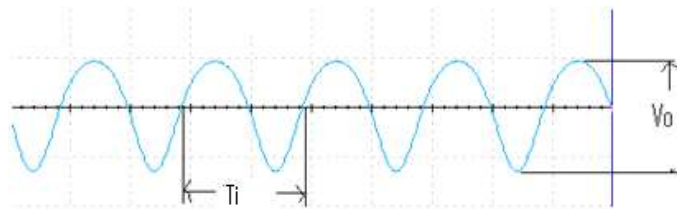


Fig.7.3 Output Wave Form of First Stage

## Second Stage Output:

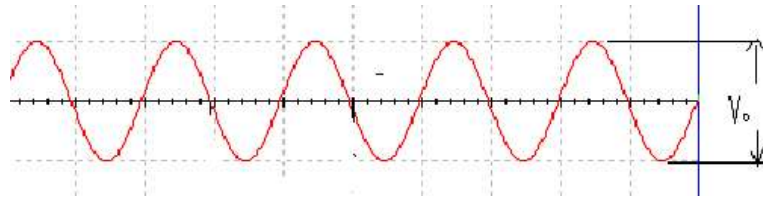


Fig.7.4 Output Wave Form of Second Stage

## Frequency Response:

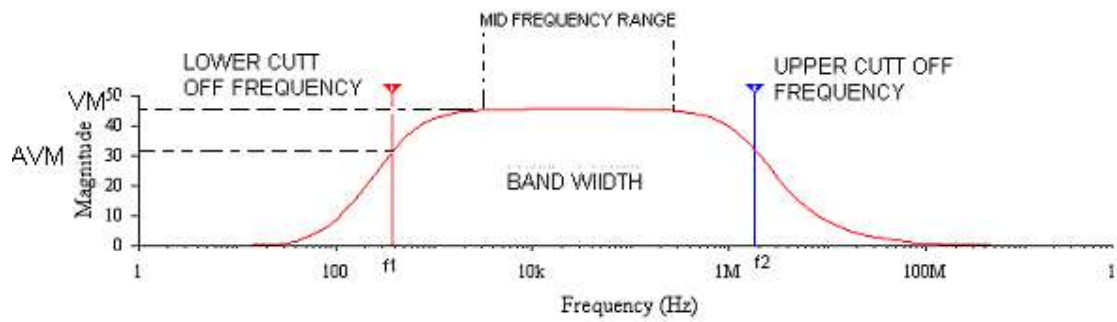


Fig.7.5 Frequency Response of RC Coupled Amplifier

## Precautions:

- 1) All connections should be tight.
- 2) Transistor terminals must be identifying properly.
- 3) Reading should be taken without any parallax error.

**Result:** Thus voltage gain is calculated and frequency response is observed along with loading affect.

## Viva Questions:

- 1) What is the necessity of cascading?
- 2) What is 3dB bandwidth?
- 3) Why RC coupling is preferred in audio range?

- 4) Which type of coupling is preferred and why?
- 5) Explain various types of Capacitors?
- 6) What is loading effect?
- 7) Why it is known as RC coupling?
- 8) What is the purpose of emitter bypass capacitor?
- 9) Which type of biasing is used in RC coupled amplifier?
- 10) What Gain of Two-Stage RC Coupled Amplifier?
- 11) What Frequency Response of Two-Stage RC Coupled Amplifier?
- 12) What is RC coupled amplifier?
- 13) How to improve the frequency response of amplifier?
- 14) What is the value of all resistor use in this experiment? Why we use them?
- 15) Which configuration is used in RC coupled amplify

## EXPERIMENT NO:-11

**Object:-**Plot drain current - drain voltage and drain current – gate bias characteristics of field effect transistor and measure of  $I_{DSS}$  &  $V_p$

### Apparatus:

S No.	Equipment	Range	Quantity
	Power supply	(0 to 30) v	1
	FET(BFW11)		1
	Resistor	1K $\Omega$	1
	Ammeters	(0-100 mA)	1
	Voltmeter	(0-20 V)	2
	connecting wires		

### Theory:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET is always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with  $V_{DS}$ . With increase in  $I_D$  the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The  $V_{DS}$  at this instant is called “pinch of voltage”.

If the gate to source voltage ( $V_{GS}$ ) is applied in the direction to provide additional reverse bias, the pinch off voltage will be decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS} (1 - V_{GS}/V_p)^2$$

## Circuit Diagram

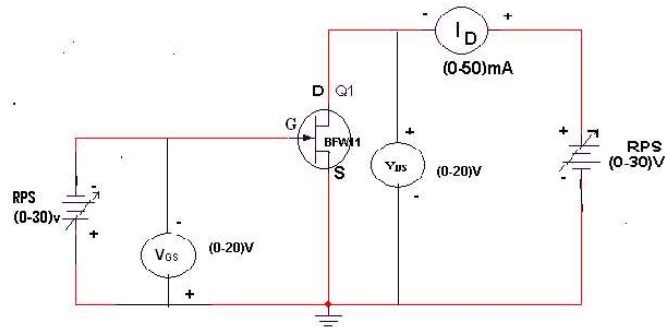


Fig.5.1 Circuit Diagram FET characteristics

## Procedure:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep  $V_{GS}$  constant at 0V.
3. Vary the  $V_{DD}$  and observe the values of  $V_{DS}$  and  $I_D$ .
4. Repeat the above steps 2, 3 for different values of  $V_{GS}$  at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep  $V_{DS}$  constant at 1V.
7. Vary  $V_{GG}$  and observe the values of  $V_{GS}$  and  $I_D$ .
8. Repeat steps 6 and 7 for different values of  $V_{DS}$  at 1.5 V and 2V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of dynamic resistance ( $r_d$ ) by using the formula

$$r_d = \Delta V_{DS} / \Delta I_D$$

11. From transfer characteristics, calculate the value of transconductance ( $g_m$ ) By using the formula

$$G_m = \Delta I_D / \Delta V_{DS}$$

12. Amplification factor ( $\mu$ ) = dynamic resistance. Trans conductance

$$\mu = \Delta V_{DS} / \Delta V_{GS}$$

**Observations:**

**Drain Characteristics:**

S.NO	$V_{GS}=0V$		$V_{GS}=0.1V$		$V_{GS}=0.2V$	
	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$

Table.5.1

**Transfer Characteristics:**

S.NO	$V_{DS}=0.5V$		$V_{DS}=1V$		$V_{DS}=1.5V$	
	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$

Table.5.2

**Model Graph:**

**Transfer Characteristics**

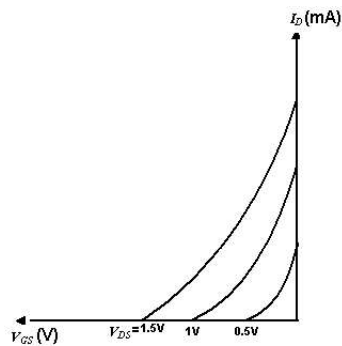


Fig.5.2 Transfer characteristics of FET

## DRAIN CHARACTERISTICS

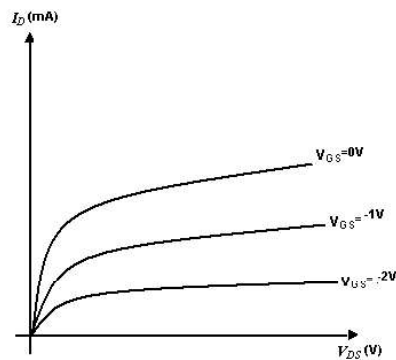


Fig.5.3 Drain Characteristics of FET

### Precautions:

1. The three terminals of the FET must be carefully identified
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltages exceeding the ratings of the FET should not be applied.

### Result:

2. The drain and transfer characteristics of a given FET are drawn
3. The dynamic resistance ( $r_d$ ), amplification factor ( $\mu$ ) and Trans conductance ( $g_m$ ) of the given FET are calculated.

### Viva Questions:

1. What are the advantages of FET?
2. Different between FET and BJT?
3. Explain different regions of V-I characteristics of FET?
4. What are the applications of FET?
5. What are the types of FET?
6. Draw the symbol of FET.
7. What are the disadvantages of FET?
8. What are the parameters of FET?



## EXPERIMENT NO:-12

**OBJECT:** To plot and study the characteristics of small signal amplifier using FET.

**Apparatus Required:** FET (BFW-11)

S No.	Equipment	Range	Quantity
1.	Dual Power supply	(0 to 30) v	1
2.	Voltmeter	(0 to 20) v	2
3.	Ammeter	(0-100mA)	1
4.	Connecting wires		
5.	FET (BFW-11)		1

### Theory:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with  $V_{DS}$ . With increase in  $I_D$  the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The  $V_{DS}$  at this instant is called “pinch of voltage”. If the gate to source voltage ( $V_{GS}$ ) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS}(1 - V_{GS}/V_P)^2$$

## Circuit Diagram

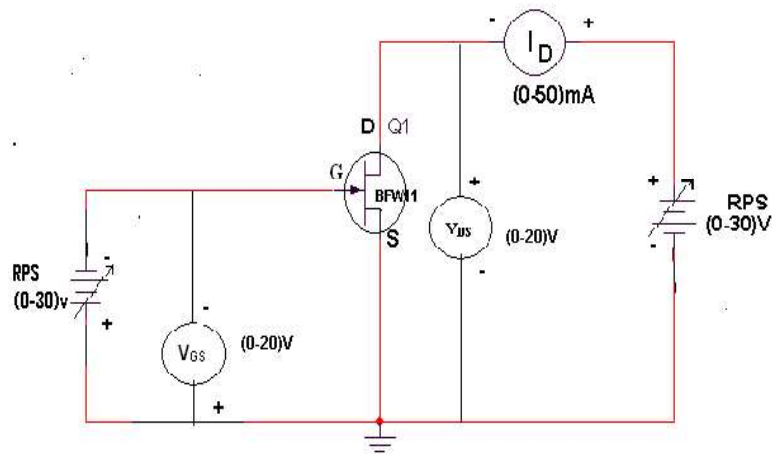


Fig 3.1 circuit diagram of FET Characteristics

### Procedure:

13. All the connections are made as per the circuit diagram.
14. To plot the drain characteristics, keep  $V_{GS}$  constant at 0V.
15. Vary the  $V_{DD}$  and observe the values of  $V_{DS}$  and  $I_D$ .
16. Repeat the above steps 2, 3 for different values of  $V_{GS}$  at 0.1V and 0.2V.
17. All the readings are tabulated.
18. To plot the transfer characteristics, keep  $V_{DS}$  constant at 1V.
19. Vary  $V_{GG}$  and observe the values of  $V_{GS}$  and  $I_D$ .
20. Repeat steps 6 and 7 for different values of  $V_{DS}$  at 1.5 V and 2V.
21. The readings are tabulated.
22. From drain characteristics, calculate the values of dynamic resistance ( $r_d$ ) by using the formula

$$r_d = \Delta V_{DS} / \Delta I_D$$

23. From transfer characteristics, calculate the value of transconductance ( $g_m$ ) By using the formula

$$G_m = \Delta I_D / \Delta V_{DS}$$

24. Amplification factor ( $\mu$ ) = dynamic resistance. Trans conductance

$$\mu = \Delta V_{DS} / \Delta V_{GS}$$

**Observations:**

**Drain Characteristics:**

S.NO	$V_{GS}=0V$		$V_{GS}=0.1V$		$V_{GS}=0.2V$	
	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$

Table 3.1

**Transfer Characteristics:**

S.NO	$V_{DS}$ $=0.5V$		$V_{DS}=1V$		$V_{DS}$ $=1.5V$	
	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$

Table 3.2

**Model Graph:**

**Transfer Characteristics**

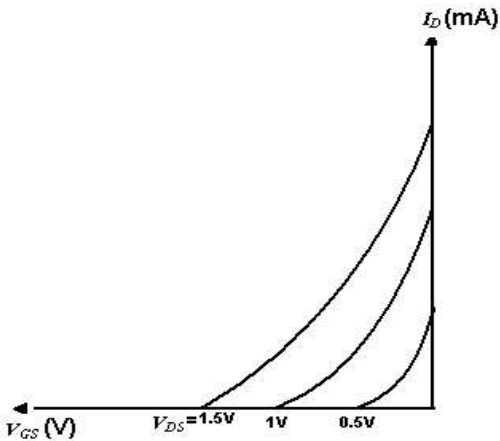


Fig 3.2 Transfer Characteristics Of Fet

**Drain Characteristics**

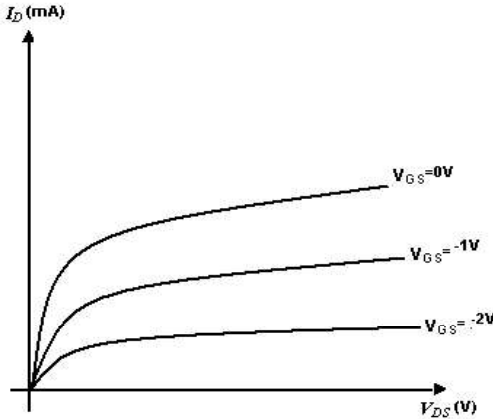


Fig 3.3 Drain Characteristics of Fet

### **Precautions:**

5. The three terminals of the FET must be carefully identified
6. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
7. Source and case should be short circuited.
8. Voltages exceeding the ratings of the FET should not be applied.

### **Result:**

The drain and transfer characteristics of a given FET are drawn

The dynamic resistance ( $r_d$ ), amplification factor ( $\mu$ ) and Trans conductance ( $g_m$ ) of the given FET are calculated.

### **Viva Quiz:**

1. Which of the following ratings appear(s) in the specification sheet for an FET?
2. What is the level of drain current  $I_D$  for gate-to-source voltages  $V_{GS}$  less than (more negative than) the pinch-off level?
3. What is the level of  $I_G$  in an FET?
4. What is the range of an FET's input impedance?
5. Which of the following applies to a safe MOSFET handling?
6. At which of the following condition(s) is the depletion region uniform?
7. What is the ratio of  $I_D / I_{DSS}$  for  $V_{GS} = 0.5 V_P$ ?
8. Which of the following controls the level of  $I_D$ ?
9. Which of the following is (are) the terminal(s) of a field-effect transistor (FET).
10. How many terminals can a MOSFET have?
11. In the constant current region, how will the  $I_{ds}$  change in an n-channel JFET

## EXPERIMENT NO:-1 (beyond syllabus)

**Object:** - To design a BJT Darlington Emitter follower and determine the gain, input and output impedances.

### Apparatus Required:

S.No.	Apparatus	Specification	Quantity
1.	Transistor	BC 547B	2
2.	Regulated power supply	0-30V	1
3.	Resistor	1K $\Omega$ 1M $\Omega$	1 1
4.	Potentiometer	100k $\Omega$	1
5.	Connecting wires	-	

### Theory:

The Darlington Pair is a useful circuit configuration for many applications within electronic circuits. The Darlington transistor configuration provides a number of advantages that other forms of transistor circuit are not able to offer and as a result it is used in many areas of electronics design. The Darlington Pair also occasionally referred to as a super-alpha pair is renowned as a method for obtaining a very high level of current gain, using just two transistors. It is able to provide levels of gain that are not possible using single transistors on their own, but it may not be used in all circumstances because it does have a number of limitations.

The Darlington Pair may be used in the form of discrete components, but there are also very many integrated circuit versions often termed a Darlington transistor that may also be used. These Darlington transistor components may be obtained in a variety of forms including those

for high power applications where current levels of many amps may be required.

The Darlington Pair has been in use for very many years. It was invented in 1953 by Sidney Darlington who was working at Bell Laboratories. He developed the idea of having two or three transistors in a single semiconductor chip, where the emitter of one transistor was connected directly to the base of the next, and all the transistors shared the same collector connection. In many ways the Darlington bore many of the hallmarks of the first integrated circuit patent, but it was too specific to the specific Darlington circuit itself to be considered as an integrated circuit.

### Circuit Diagram:

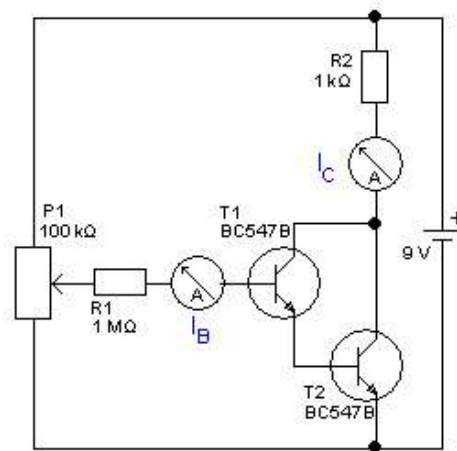


Fig 1.1 circuit Diagram of arlington Emitter follower

### Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set  $V_i = 1$  volt (say), using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

## General Procedure for Calculation:

### 1.1 Input impedance

- a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).
- b. Connect ac voltmeter (0-100mV) across the biasing resistor  $R_2$ .
- c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.
- d. Note down the resistance of the DRB, which is the input impedance.

### 1.2. Output impedance

- a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected ( $V_{load}$ ).
- b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ( $V_{no-load}$ ).
- c. Substitute these values in the formula  $Z_O = V_{load} - V_{no-load} \cdot 100\%$

$$V_{load}$$

### 1.3. Bandwidth:

- a. Plot the frequency response
- b. Identify the maximum gain region.
- c. Drop a horizontal line at -3dB.
- d. The -3dB line intersects the frequency response plot at two points.
- e. The lower intersecting point of -3dB line with the frequency response plot gives the lower cut-off frequency.
- f. The upper intersecting point of -3dB line with the frequency response plot gives the upper cut-off frequency.
- g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth =  $f_h - f_l$ .



### 1.4. To find Q-Point

- Connect the circuit as per circuit diagram
- Switch on the DC source [switch off the AC source]
- Measure voltage at  $V_{B2}$ ,  $V_{E2}$  &  $V_{C2}$  with respect to ground

& also measure

$$V_{CE2} = V_{C2} - V_{E2}$$

$$I_{C2} = I_{E2} = \frac{V_{E2}}{R_E}$$

$$Q - \text{Point} = [V_{CE2}, I_{C2}]$$

### Observation Table:

S.NO	FRQUENCY	V <sub>IN</sub> (Volt)	V <sub>O</sub> (Volt)	Gain = V <sub>O</sub> /V <sub>i</sub>	Gain(dB) =20log V <sub>O</sub> /V <sub>i</sub>

Table 1.1

### Frequency Response

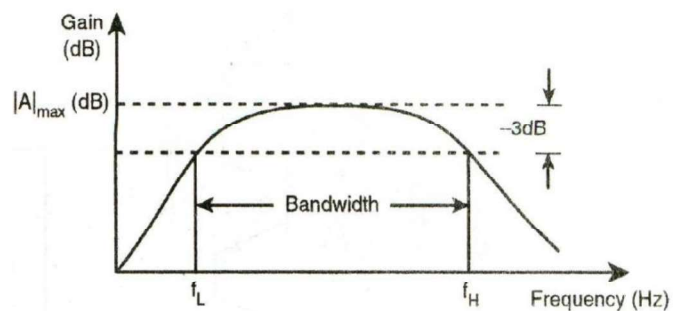


Fig 1.2 Frequency Response of Darlington Emitter follower

## Result.

	Theoretical	Practical
<b>Input Impedance</b>		
<b>Output Impedance</b>		
<b>Gain (Mid Band)</b>		
<b>Bandwidth</b>		

Table 1.2

## Viva questions:-

1. What is Darlington pair?
2. What are the advantages of Darlington pair?
3. How does the Darlington pair operate?
4. What did you mean by Darlington pair?
5. What is the V I characteristics of a Darlington pair?
6. What is the input impedance of Darlington emitter follower?
7. What are the difference between Darlington pair characteristics and Darlington emitter follower characteristics?
8. What is mid frequency gain of Darlington emitter follower?
9. What is the output impedance of Darlington emitter follower?
10. What is the application of Darlington pair?
11. Draw the circuit diagram of Darlington pair?
12. What is the use of resistance  $R_1$  and  $R_2$  in the Darlington pair circuit?
13. What will the effect if both transistors are not same type in the circuit?
14. What will be the out put at collector terminal of transistor  $T_1$ ?
15. What will be the input at base terminal of transistor  $T_2$ ?

## EXPERIMENT NO:-2 (beyond syllabus)

**Object:-**To determine regulation characteristics of voltage doublers.

### Apparatus Required:

S. No.	Apparatus Required	Range	Quantity
1.	RPS	(0 – 30) V	1
2.	Transformer	(6-0-6) V	1
3.	Diode	IN4001	2
4.	Capacitor	100 $\mu$ F	1
5.	Resistor	10 K $\Omega$ , 100K $\Omega$	1 1
6.	DC Voltmeter	(0-30) V	1
7.	Ammeter	(0-50) mA	1
8.	CRO	--	1
9.	FGR	--	1
10.	Bread Board	--	1
11.	Connecting Wires	--	15

### Theory:

It is a clamper circuit. A voltage doubling circuit produces an output voltage which is approximately double the peak voltage of the input waveform. When the point 'A' is positive with respect to point 'B' diode D1 conducts and capacitor C1 is charged to the maximum voltage  $V_m$  of the applied A.C voltage in the polarity. When the point 'B' is positive relative to point A, diode D2 conducts and capacitor C2 is charged to the maximum voltage.  $E_m$  in the polarity shown.

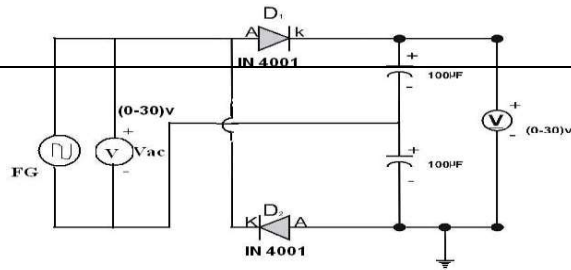


Fig 2.1 circuit Diagram of voltage doubler

### Procedure:

1. Connections are made as shown in the circuit diagram.
2. Power supply is switched ON
3. The full load is applied until the ammeter shows the rated value
4. Remove the load and take ammeter , voltmeter readings
5. Varying the Rheostat load at various point at ammeter ant
6. corresponding reading are taken and tabulated
7. Graph is plotted between dc current and dc voltage reading.

### Tabulation:-

Signal	Input Signal		Output Signal	
	Amplitude (v)	Time (ms)	Amplitude (v)	Time (ms)

Table 2.1

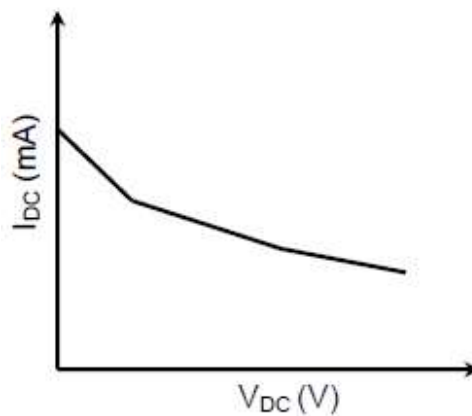


Fig 2.2 Curve between  $V_{dc}$  and  $I_{dc}$

**Application:**

1. Used in AC and DC radio receivers.
2. Used in other devices where use of power transformer is not permitted.
3. Used in power supplies for X ray tubes.
- 4.

**Result:** Thus the characteristics of Voltage Doublers Circuits were constructed and studied and its input and output waveforms were drawn.

**VIVAQUESTIONS:-**

1. What is the application of voltage doublers?
2. What is the difference between voltage doublers and voltage triplers?
3. What will be the output of voltage doublers?
4. What is the use of capacitor in the circuit?
5. Draw the circuit diagram of voltage triplers?
6. Draw the circuit diagram of voltage quadruple?
7. What is the difference between voltage quadruple and voltage triplers?
8. What is the application of voltage triplers?
9. What is the application of voltage quadruple?
10. What is the main application of voltage multiplier?
11. What is the significance of voltage multiplier circuit?
12. What is the type of voltage multiplier?
13. Are only polar capacitors used in voltage multipliers?
14. What is the voltage control voltage source?
15. What will the output of the voltage doublers?