**Techno India NJR Institute of Technology**



**Course File**

**Computer Architecture (5EC3-01)**

**Session 2023-24**

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**Course Overview:**

To study concepts related to Computer Data Representation, Micro-operations, Instructions, Programming the basic computer, Central Processing Unit, Computer Arithmetic, Memory Organization, Multiprocessors etc. which is vital to excel in the field of Computer Architecture domain.

**Course Outcomes:**

|  |  |  |
| --- | --- | --- |
| **CO.NO.** | **Cognitive Level** | **Course Outcome**  |
| 1 | **Comprehension** | Develop an ability to understand the design and interconnection of various parts of a computer |
| 2 | **Application** | Develop an ability to understand and apply the basic computer arithmetic operations |
| 3 | **Synthesis** |  Design & Develop interfacing circuitry an ability memories and input/output organization to CPU. |
| 4 | **Learning** | Learn the different types of serial communication techniques. |
| 5 | **Summarize** | Summarize the Instruction execution stages. |

**Prerequisites:**

1. Fundamentals knowledge of Binary Number System.
2. Fundamentals knowledge of Combinational Circuit.
3. Fundamentals knowledge of Sequential circuit.

**Course Outcome Mapping with Program Outcome:**

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| --- | --- |
| **Course Outcome**  | **Program Outcomes (PO’s)** |
| **CO. NO.** | **Domain Specific**  | **Domain Independent**  |
|  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| CO1 | 2 | 2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| CO2 | 2 | 2 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| CO3 | 2 | 1 | 2 | 2 | 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| CO4 | 2 | 2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| CO5 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1: Slight (Low) , 2: Moderate (Medium), 3: Substantial (High)  |

**Course Coverage Module Wise:**

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| **Lecture No.** | **Unit** | **Topic** |
|  | **1** | **INTRODUCTION: COMPUTER ARCHITECTURE** |
|  | 1 | Objective, scope and outcome of the course. |
|  | **2** | **BASIC STRUCTURE OF COMPUTERS** |
|  | 2 | Functional units, software, performance issues software,  |
|  | 2 | Machine instructions and programs |
|  | 2 | Types of instructions, Instruction sets: Instruction formats, |
|  | 2 | Assembly language, Stacks, Ques, Subroutines. |
|  | **3** | **PROCESSOR ORGANIZATION, INFORMATION REPRESENTATION** |
|  | 3 | Number formats. Multiplication & division, ALU design |
|  | 3 | Floating Point arithmetic, IEEE 754 floating point formats |
|  | 3 | Control Design |
|  | 3 | Instruction sequencing |
|  | 3 | Interpretation |
|  | **4** | **HARD WIRED CONTROL DESIGN METHODS AND CPU CONTROL UNIT.** |
|  | 4 | Microprogrammed Control - Basic concepts |
|  | 4 | Minimizing microinstruction size |
|  | 4 | Multiplier control unit |
|  | 4 | Microprogrammed computers - CPU control unit |
|  | **5** | **MEMORY ORGANIZATIONS** |
|  | 5 | Device characteristics, RAM, ROM, Memory management |
|  | 5 | Concept ofCache & associative memories, |
|  | 5 | Virtual memory. |
|  | **6** | **SYSTEM ORGANIZATION, INPUT - OUTPUT SYSTEMS** |
|  | 6 | Interrupt, DMA |
|  | 6 | Standard I/O interfacesConcept of parallel processing |
|  | 6 | Pipelining |
|  | 6 | Forms of parallel processing |
|  | 6 | Interconnect network |

**TEXT/REFERENCE BOOKS**

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| 1. Morris M. Mano, Computer Systems Architecture.3 ed, Prentice Hall India.
2. Carl Hamachar and Vranesic, Computer Organization, McGraw Hill.
3. John P. Hayes, Computer Architecture and Organization, TMH.
4. William stalling, Computer Organization and architecture, Pearson education.
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| **NPTEL COUSES LINK**1. https://nptel.ac.in/courses/106/105/106105163/
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| **QUIZ Link** 1. https://www.sanfoundry.com/1000-computer-organization-architecture-questions-answers/
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**Assessment Methodology:**

1. Two Midterm exams where student have to showcase subjective learning.
2. Final Exam (subjective paper) at the end of the semester.



